Preface

This is a first book on the topic of reconfigurable network-on-chip, which is a culmination of growing trends in the two hot research areas, namely reconfigurable computing and network-on-chip. While reconfigurable computing has brought immense flexibility in on-chip processing, network-on-chip has brought similar flexibility in on-chip communication. The integration of these two areas of research will reap the benefits of both and is a promising future design paradigm for multiprocessor systems-on-chip.

Design issues related to reconfigurable network-on-chip are numerous, some of which include the following. How reconfigurable computing techniques are to be integrated into the network-on-chip design flow? How must one reconfigure the processing elements attached to a network-on-chip? How must one design a reconfigurable router? How must a set of given tasks be assigned to the processing elements? How must one schedule the arrival of tasks or the configuration of processing elements in a network-on-chip? How can one leverage reconfiguration techniques to avoid crosstalk interferences in a network-on-chip? How can one design low-power network-on-chip using reconfiguration techniques? How can one design a programming model for the processing elements attached to a network-on-chip? How can an operating system be designed to take advantage of the computing and communication flexibilities brought about by run-time reconfiguration and network-on-chip? The above list is just a partial one and from this one can guess the importance of a book like this. This is the single reference, where most of the above issues will be discussed and elaborated on.

Since most of the above design issues are still in the research and development stage. This book presents the state-of-the-art techniques that can handle the integration of reconfiguration and network-on-chip. Besides a description of the techniques, the book also describes specific application domains where the techniques have actually been applied with success. Thus, the book can be seen as a collection of techniques and applications for reconfigurable network-on-chip.

The book can be used by students, researchers, and engineers. Students interested in reconfigurable system design, network-on-chip, system-on-chip, multiprocessor design, router design, parallel computing should be interested in this book because it can provide reference materials to study all the mentioned topics. This book is recommended for researchers interested in solving the design issues related to network-on-chip and reconfigurable systems. Last but not the least, engineers will find a wealth of techniques and applications in this book related to network-on-chip and reconfigurable system design.

The book is basically divided into five sections as follows:
SECTION 1: INTRODUCTION TO RECONFIGURABLE NETWORK-ON-CHIP

This section introduces reconfigurable network-on-chip from the design perspective, including a summary of all the issues and possible solutions. It also discusses the design of reconfigurable routers and network interfaces. This section has four chapters.

• **The chapter titled:** “A NoC-Based Infrastructure to Enable Dynamic Self Reconfigurable Systems” by Möller, Grehs, Carvalho, Soares, Calazans, and Moraes from Brazil describes how a reconfigurable NoC architecture is designed and two proof-of-concept examples illustrate the proposed architecture. The design consists of both hardware and software parts.

• **The chapter titled:** “Dynamically Reconfigurable Networks-on-Chip using Runtime Adaptive Routers” by Véstias and Neto from Portugal describes how reconfigurable routers may be designed for reconfigurable NoCs. Static and runtime adaptive routers are compared and it is shown that runtime adaptive routers are essential for today’s complex system-on-chip designs.

• **The chapter titled:** “Keys for Administration of Reconfigurable NoC: Self-Adaptive Network Interface Case Study” by Dafali and Diguet from France describes the relation between reconfigurable NoC and the OSI network layers. Further, dynamic reconfiguration administration, network infrastructure reconfiguration and network protocol reconfiguration are all discussed. A self-adaptive network interface architecture is also proposed.

• **The chapter titled:** “An Efficient Hardware/Software Communication Mechanism for Reconfigurable NoC” by Lin, Shen, and Hsiung from Taiwan proposes three communication architectures for interconnecting an NoC with a microprocessor bus-based conventional architecture. It is shown that the shared memory approach is a good tradeoff between performance and memory space consumption.

SECTION 2: DESIGN METHODS FOR RECONFIGURABLE NOC DESIGN

This section is mainly about modeling and design methods for reconfigurable NoC. This section consists of three chapters.

• **The chapter titled:** “Design Methodologies and Mapping Algorithms for Reconfigurable NoC-Based Systems” by Rana, Santambrogio, and Meroni from Italy discusses a tile-based approach to reconfigurable NoC architecture design. Existing architectures are leveraged for the development of reconfigurable NoC architecture.

• **The chapter titled:** “From MARTE to Reconfigurable NoCs: A Model Driven Design Methodology” by Quadri, Elhaji, Meftali, and Dekeyser from France describes the adaptation of MARTE, an OMG standard for real-time and embedded systems, to complex NoC-connected partially dynamically reconfigurable systems.

• **The chapter titled:** “Dynamic Reconfigurable NoCs: Characteristics and Performance Issues” by Rana, Santambrogio, and Corbetta from Italy describes the design and implementation issues for reconfigurable NoC such as the placement of bus macros for connecting static and reconfigurable parts of the NoC. A layered approach is also presented for solving switching, routing, and communication protocol design issues.
SECTION 3: HIGH-LEVEL PROGRAMMING OF RECONFIGURABLE NOC-BASED SOCS

This part discusses how NoC-based system-on-chip is to be programmed. This section contains only one chapter.

- **The chapter titled:** “High-Level Programming of Dynamically Reconfigurable NoC-Based Heterogeneous Multicore SoCs” by Vanderbauwhede from UK describes Gannet, a programming model and framework which makes software and hardware integration easier. The inherent parallelism and dynamic reconfigurability can be fully utilized by a user programming with Gannet.

SECTION 4: SIMULATION FRAMEWORK FOR FAST RECONFIGURABLE NOC EMULATION

This section is mainly about how NoC can be emulated. This section consists of only one chapter.

- **The chapter titled:** “Dynamic Reconfigurable NoC (DRNoC) Architecture: Application to Fast NoC Emulation” by Krasteva, de la Torre, and Riesgo from Spain describes an emulation method for exploring the different communication design alternatives corresponding to adapting routers, network interfaces, and processing cores.

SECTION 5: STATE-OF-THE-ART RECONFIGURABLE NOC DESIGNS

This section consists of four examples on different reconfigurable NoCs. Some of them focus on power reduction, some on crosstalk reduction, and yet another on how topology is adapted.

- **The chapter titled:** “Dynamically Reconfigurable NoC for Future Heterogeneous Multi-Core Architectures” by Ahmad, Ahmadinia, and Arslan from UK describes how hardware reconfigurability can be exploited in terms of switching, routing, and packet size. A new architecture for reconfigurable NoC is proposed and evaluated against fixed NoCs.

- **The chapter titled:** “Reliability Aware Performance and Power Optimization in DVFS-Based On-Chip Networks” by Yanamandra, Eachempati, Narayanan, and Irwin from USA proposes a dynamically reconfigurable data protection scheme in NoC, while minimizing power and performance overheads. This is an increasingly important topic due to the variations in chip fabrication brought about by deep-submicron technologies. NoC being a data communication mechanism must support such protection schemes. Reconfigurability further enhances this protection scheme by providing both flexibility and cost reduction.

- **The chapter titled:** “SpaceWire Inspired Network-on-Chip Approach for Fault Tolerant System-on-Chip Designs” by Osterloh, Michalik, and Fiethe from Germany proposes a specialized NoC architecture that can withstand the disruption effects of radiation induced particles in space. This is a very interesting application domain in which dynamically reconfigurable NoC technology brings
all the advantages that were unforeseen before in this area. High reliability is a critical issue in this
domain and reconfigurable NoC can be leveraged to achieve this.

- **The chapter titled:** “A High-Performance and Low-Power On-Chip Network with Reconfigurable Topology” by Modarressi and Sarbazi-Azad from Iran proposes an NoC with reconfigurable topology such that it can be configured dynamically to fit the traffic pattern requirements of a set of applications. Experiments demonstrate the performance improvement and power reduction brought about by such an adaptation scheme between topology and traffic pattern.

This book is a collective effort by a group of expert representatives in the area of reconfigurable network-on-chip design. We believe that the technologies, issues, and solutions presented in this book will be of immense help to researchers and engineers in various fields of application such as real-time embedded systems, system-on-chip, multimedia, and networking.

The integration of reconfigurable computing techniques and network-on-chip communication infrastructure is inevitable. This book provides a basic reference for such an integration. Though there are still lots of research issues to be solved in this integration, we are already at a stage where we need more convergence on how our technologies have affected this well-known communication structure.

Any queries related to this book can be addressed to one of the authors.

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