

# Index

256-bit Barreto-Naehrig curves 96  
 3rd Generation Partnership Project (3GPP) 122, 139

## A

Abstract Machine Notation (AMN) 303  
 action systems 45, 49, 221  
 Adaptive Logic Modules (ALM) 161  
 Adaptive Look-Up Tables (ALUT) 161  
 Address Generation Units (AGU) 111  
 Advanced Encryption Standard (AES) 19, 124, 139  
 Analog Front-End (AFE) 105  
 application modeling 263, 265, 275  
 Application Programming Interface (API) 61, 66, 242  
 Application-Specific Instruction-set Processors (ASIP) 79  
 Application-Specific Integrated Circuit (ASIC) 103, 157  
 Architectural Modeling Programming Interface (AMPI) 125  
 Architecture Description Language (ADL)  
   mixed ADLs 81  
   behavioral ADLs 81  
   structural ADLs 81  
 Architecture Description Languages (ADL) 79  
 ARM1176 embedded processor 124  
 asynchronous communication 220  
 asynchronous communication handshake 224  
 asynchronous connectors 227  
 asynchronous pull channel 225-226  
 asynchronous push channel 225

## B

Behavioral Address Coding Template (BACT) 37  
 Bit Error Rate (BER) 147, 151  
 B method 298, 302  
 Broadcast Channel (BCCH) 129  
 butterfly fat-tree topology 237

## C

Category four User Equipment (CAT4 UE) 102  
 cell processor 60-61, 77  
 Channel Access Functions (CAF) 247-248, 257  
 channel access protocol 247  
 channel buffer 247-249, 253  
 channel control variables 247  
 Channel Preprocessor Unit (ChPU) 112  
 Channel Quality Indication (CQI) 109  
 Code Division Multiple Access (CDMA) 103  
 Common Control Channel (CCCH) 129  
 Communicating Sequential Processes (CSP) 239, 265  
 communication service 198  
 communication structures 178, 180, 191  
 competing relationship  
   direct 203  
   indirect 203  
 Complex-valued Multiply-and-ACcumulate (CMAC) 112  
 component allocation 242  
 component-based design 246  
 components and agents 286  
 computation unit 45  
   resource 46  
 conflict free memory access 39  
 cryptographic pairings 95-96, 98-99  
 cryptosystems 5

## D

data security 5  
 Dedicated Control Channel (DCCH) 130  
 Dedicated Traffic Channel (DTCH) 126  
 Deep Sub-Micron (DSM) 178, 183, 195  
 design-space exploration 80, 93, 96  
 design verification 15  
 Device Interconnect Protocol (DIP) 148

device interoperability 4  
Dhrystone benchmark application 128, 132  
Diagnostic and Adaptivity Processing (DAP) 279  
Differential Power Analysis (DPA) 17  
Digital BaseBand (DBB) 105, 109, 123  
Digital Front-End (DFE) 105, 109  
Digital Signal Processor (DSP) 157  
Digital Video Broadcasting (DVB) 106, 158  
Direct Memory Access (DMA) 26, 59-60, 124  
direct monitoring 288  
Distributed System Object (DSOC) 245  
Double Data Rate (DDR) 82  
Downlink Shared Channel (DLSCH) 127

## E

electronic systems  
  gigascale 2  
  nanoscale 2  
Element Interconnect Bus (EIB) 61  
embedded networks 143, 149, 151, 153  
embedded security 5  
Embedded System-level Platform synthesis and Application Mapping (ESPAM) 245  
embedded systems 1-3, 6, 14, 16  
encryption keys 6  
energy-awareness 44-45, 50

## F

fault tolerance 308  
Field Programmable Gate Array (FPGA) 156  
Finite State Machine (FSM) 265, 270  
First-In First-Out (FIFO) 65, 113  
Forward Error Correction (FEC) 103  
Frequency Division Duplexing (FDD) 103

## G

Globally Asynchronous Locally Synchronous (GALS) 178, 220  
Graphical User Interface (GUI) 161  
Gray Level Co-occurrence Matrix (GLCM) 60

## H

H.264 Motion Compensation 59, 67  
Hardware Description Language (HDL) 80, 156, 246  
hardware/software co-design 123  
HERMES 268  
Hierarchical Agent Monitored SoCs (HAMSOC) 278, 280-281

Hybrid Automatic Repeat ReQuest (H-ARQ) 103  
Hyper Frame Number (HFN) 130

## I

input variables 222  
Integrated Signal processing Systems (ISS) 81

## K

Kahn Process Network (KPN) 242

## L

Large Scale Integration (LSI) 6, 21, 99  
level of detail 267  
Link Failure Probability (LFP) 179, 194-195  
Log-Likelihood Ratio (LLR) 114  
Long-Term Evolution (LTE) 102-103, 122  
Lyra method 297-299  
  service decomposition phase 300  
  service distribution phase 301  
  service implementation phase 302  
  service specification phase 299

## M

macroblock (MB) decoding 68  
macroblock (MB) partition 68  
Medium Access Control (MAC) 126, 139  
Memory-Access Timing Model 84  
Memory-Access Unit (MAU) 94-95  
Memory Flow Controller (MFC) 62  
memory interface 79-82, 92, 98  
memory-interface controller 86-89, 92  
Memory-Interface Description (MID) 80, 86, 88  
  behavioral elements 87  
  structural elements 86  
Memory-Interface Intermediate Representation (MIIR) 89  
memory mapping 90, 92-93  
memory-resource specific external interface 85-86  
memory subsystem 26  
  design 28  
memory types  
  asynchronous 82  
  dynamic 83  
  pipelined 83  
  static 83  
  synchronous 82  
mesh connected crossbar architecture 237  
MIDdleware based on Action Systems (MIDAS) 45  
middleware level 44

Minimum Mean-Square-Error (MMSE) 107  
 Minimum Sized Inverters (MSI) 181-182, 188  
 model confidence 267  
 Model of Computation (MoC) 242  
 Models of Computation (MoC) 154, 265  
 monitoring operations 288  
     specifications 290  
     types 288  
 Motion Compensation (MC) 59-60, 67, 77-78  
 Motion Vector Prediction (MVP) 60, 68  
 Motion Vectors (MV) 60, 68  
 Multidimensional Software Cache (MDSC) 59-61, 64, 76  
 Multiple-Input Multiple-Output (MIMO) 103  
 Multi-Processor System-on-Chip (MPSoC) 6, 79, 156, 173, 220, 263

## N

network latency  
     basic 202  
     latency analysis 198  
     upper bound analysis 204, 209  
 network manager 44  
 Network-on-Chip (NoC) 11, 16, 20, 154, 158, 163, 178, 195, 197-198, 217-218, 263, 276-278, 281, 295  
 Next Iteration Initialization (NII) 113  
 nonregime 1  
 NoTA 148

## O

Open Computing Language (OpenCL) 24  
 Orthogonal Frequency Division Multiple Access (OFDMA) 103  
 output variables 222

## P

Packet Data Convergence Protocol (PDCP) 126, 139  
 Paging Control Channel (PCCH) 129  
 Parallel Memory Coding Template (PMCT) 40  
 parallel programming 24, 37  
 Payload Abstraction Technique (PAT) 267, 270  
 photogrammetry logic 273  
 Physical Downlink Shared-Channel (PDSCH) 105  
 PHY solution 147  
 PHY technology 147  
 Platform Abstraction Layer (PAL) 243-244, 249  
 platform modeling 267  
     BOÇA 270

JOSELITO 268  
 RENATO 268  
 platform topology 242  
 power monitoring 291, 293  
 Power Processor Element (PPE) 61  
 Pre-coding Matrix Indication (PMI) 109  
 Primary Synchronization Signal (PSS) 105  
 Printed Wiring Board (PWB) 144  
 processor architecture 79, 82  
 Process, Voltage and Thermal (PVT) 279  
 prolog and epilog 25  
 Protocol Data Unit (PDU) 128  
 protocol processing 123-124

## Q

Quadratic Permutation Polynomial (QPP) 115  
 Quality-of-Service (QoS) 11, 147, 149, 153, 276

## R

radio baseband 110  
 Radio Link Control (RLC) 105, 126, 139  
 Random Dopant Fluctuation (RDF) 177, 179, 196  
 Real-Time Operating System (RTOS) 123, 128, 131  
 Register Transfer Level (RTL) 10, 55, 79-80, 246  
 remote monitoring 288  
 Retinex algorithms 96  
 Robust Header Compression (ROHC) 126, 140

## S

schedulability analysis 198, 200  
 scratchpad memory 60, 68  
     software cache 60  
 Secondary Synchronization Signal (SSS) 105  
 self-aware systems 4  
 service availability analysis 251  
 Service Data Units (SDU) 128  
 service dependency graph 246  
 service exchange relations 249  
 service export relations 250  
 service flow graph 251  
 service import relations 250  
 Service Relation Model (SRM) 244, 249  
 Single-Carrier Frequency Division Multiple Access (SC-FDMA) 104  
 Single Instruction Multiple Data (SIMD) 62  
 Single Instruction Multiple Task (SIMT) 35, 110  
 Single Processor System-on-Chips (SPSoC) 8  
 Soft-Input Soft-Output (SISO) 113

## ***Index***

Software Defined Radio (SDR) 16, 102-103, 110, 120, 157  
stepwise refinement 220  
StratixII and StratixIV 156  
sustainable development 45  
Symmetric Multi-Processing (SMP) 245  
Synchronous Data Flow (SDF) 265  
Synergistic Processing Elements (SPE) 61  
Synergistic Processing Unit (SPU) 62  
System-on-Chip (SoC) 8, 14, 16, 19, 79, 123, 138, 156, 173-175, 178, 264-265  
System-on-Package (SoP) 8

### **T**

tapered buffers 180, 185  
Task-Transaction Level (TTL) 245  
Time Division Duplexing (TDD) 103  
Transmission Time Interval (TTI) 128, 132, 134

### **U**

UML sequence diagram 265  
unified internal interface 85

Unified Modeling Language (UML) 264, 298, 319

UniPro proposal 147

Universal Asynchronous Receiver Transmitter (UART) 124

Universal Serial Bus (USB) 16, 155

### **V**

vector memory 24, 28-30, 40

Vector Register File (VRF) 24, 26, 28-29, 31-33, 35, 38-39

very large scale integration (VLSI) 6, 21, 99

virtual hardware platform 123

Virtual System Prototype (VSP) 123-124, 131, 136

### **W**

Wireless Local Area Networks (WLAN) 5

wormhole switching 199

  communication 199

  priority based 200, 204

  schedulability 199