Integration of Optimization Approach Based on Multiple Wordlength Operation Grouping in the AAA Methodology for Real-Time Systems: LVQ Implementation

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ABSTRACT

The Multiple-Wordlength Operation Grouping (MWOG) is a recently used approach for an optimized implementation on a Field Programmable Gate Array (FPGA). By fixing the precision constraint, this approach allows minimizing the data wordlength. In this paper, the authors present the integration of the approach based on the MWOG in the Algorithm Architecture Adequation (AAA) methodology, designed to implement real-time applications onto reconfigurable circuits. This new AAA-MWOG methodology will improve the optimization phase of the AAA methodology by taking into account the data wordlength and creating approximative-wordlength operation groups, where the operations in the same group will be performed with the same operator. The AAA-MWOG methodology will allow a considerable gain of circuit resources. This contribution is demonstrated by implementing the Learning Vector Quantization (LVQ) neural-networks model on the FPGA. The LVQ optimization is used to quantify vigilance states starting from processing the electroencephalographic signal. The precision-gain relation has been studied and reported.

Keywords: Adequacy Algorithm Architecture, Multiple-Wordlength Operation Grouping, LVQ Neural Networks, Optimized Implementation, Precision Constraint

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INTRODUCTION

The main objective of hardware implementation is to find the optimal design in terms of area while respecting time and precision constraints. Data wordlength is one of the parameters that influences these metrics. Unlike specialised general-purpose processors, Field Programmable Gate Array (FPGA) implementations allow a number of arithmetic resources for each type (adder, multiplier, etc) and an input/output operation wordlength to be freely chosen, hence providing an important optimization potential.

In order to optimize the hardware implementation in terms of resources, it has been necessary to implement an architecture design methodology on FPGA supports. This methodology allows generating a circuit from the behavior and wordlength of the application to be implemented by exploring the design space and finding the optimized design.

Several optimized implementation methodologies on FPGA are proposed (Kaouane, 2004; Herve, 2005; Xu, 2005). These methods seek the best solution by adopting an optimization approach while respecting the objectives and constraints of the application.

We consider two classes of optimization approaches. The approaches of the first class aim at minimizing the resources for a maximum accuracy by adopting a precision study (Kum & Sung, 2001; Xu, 2005; Herve, 2005; Wadekaret, 1998). Among these approaches, some seek to use the grouping of operations that will be performed on the same operator. Grouping can be performed according to the dependencies between operations, the knowledge of the wordlength of each operation, and the sharing of known resources.

In (Herve, 2005), the authors proposed an iterative approach based on coupling the architecture synthesis and data-wordlength optimization. Indeed, the optimization required a knowledge of grouping the operations obtained by the architecture synthesis, which involved knowing the number of bits of the operations obtained by the optimization process.

In (Xu, 2005), the authors suggested synthesizing the multiple-width architecture and optimizing the data flow graph of the application while minimizing the data flow graph after generating the operations’ wordlength. A cost function was a functional unit that combined a set of operations on the application according to the dependencies between operations.

In (Kum & Sung, 2001), the authors put forward a method of a multiple-width architecture synthesis characterized by an initial synthesis phase to take advantage of both the information about resource sharing and the associated dependencies of the signal flow graph. Subsequently, a group of operations would be performed prior to the accuracy optimization phase.

In (Wadekaret, 1998), the authors adopted an optimization approach which allowed determining the operations’ wordlength, then grouping the approximative-wordlength operations and selecting the effective wordlength, and finally predicting the minimum number of resources that could be used for a group of operations.

This approach class often offers a better optimization in terms of consumed resources in achieving a precision study to identify the optimal number of bits for all data.

The approaches of the second class have not given any importance to the precision constraint, certainly leading to a minimum performance and high resource consumption. Among these approaches, some have only focused on minimizing and simplifying expressions (Hamed, 2004). Others are based on loop unrolling, taking into account the data dependencies (So, 2003; Kaouane; 2004, Niang, 2007). These approaches tend to generate circuits that fulfill the application’s real-time constraints while minimizing the amount of resources allocated for its implementation.

In (Kaouane, 2004), the authors adopted the Algorithm Architecture Adequation (AAA) methodology that would explore the solution space by graph transformations to achieve an optimal implementation respecting the time constraint.
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