Chapter 7
On the Reliability of Post-CMOS and SET Systems

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ABSTRACT

The necessity of applying fault-tolerant techniques to increase the reliability of future nano-electronic systems is an undisputed fact, dictated by the high density of faults that will plague the chips. The averaging and thresholding fault-tolerant technique that has proven remarkable efficiency in CMOS is presented for SET-based designs. Computer simulations demonstrate the superiority of this fault-tolerant technique over other methods, which is specifically the case when an adaptable threshold is used.

INTRODUCTION

The advent of ubiquitous electronic appliances in the modern information society has founded its success on the premise of using highly reliable components in every development level. Based on the mature CMOS fabrication process, larger and faster, but also power-hungry and very complex integrated circuits have been fabricated on the assumption of very reliable operation of their constituting modules, from the atomic elements such as transistors, and passive components such as capacitances, routing lines, etc., to complex modules made of several thousand of transistors, such as arithmetic and logic unit modules, memory blocks. Also, the availability of reliable electronic design automation (EDA) tools and efficient design-flows has been assumed.

The vast majority of microelectronic developments presented nowadays uses the well-established CMOS process and fabrication technology which exhibit high reliability rates. The hypothesis of reliable components has mostly been adopted in the development of electronic systems fabricated in the past four decades. Several indicators show that future fabrication processes will exhibit increased failure rates and degraded fabrication yield. This Chapter focuses on the construction of
reliable nanoelectronic systems made of intrinsically unreliable atomic constituting elements. The main sources of faults are described in Section Reliability and yield in post-CMOS fabrication technologies. In Section single electron transistors (SETs), the basic concepts and modes of operation of SETs is described. Section Techniques for improving reliability focuses on currently applied methods for increasing design reliability. The averaging and thresholding technique is presented as a method enabling increasing the reliability of nanoelectronic systems in Section Averaging and thresholding for increasing reliability. This work focuses on the specific case of single-electron transistor-based designs. The analytical framework of the averaging and thresholding technique using single-electron transistor-based designs is presented. The proposed fault-tolerant averaging and thresholding technique is compared with other standard fault-tolerant techniques in Section Comparison of different fault-tolerant techniques, showing its clear superiority in terms of fault resilience.

RELIABILITY AND YIELD IN POST-CMOS FABRICATION TECHNOLOGIES

Some typical physical defects in VLSI chips include:

- **Process defects**: missing contact windows, parasitic transistors, oxide breakdown, etc.
- **Material defects**: bulk defects (cracks, crystal imperfections), surface impurities, etc.
- **Aging defects**: dielectric breakdown, electromigration, etc.

Errors are traditionally categorized into three main groups: permanent, intermittent and transient errors according to their stability and concurrence. Permanent errors are irreversible physical changes in a chip. The most common sources for this kind of errors are the manufacturing processes. Permanent errors also occur during usage lifetime of the circuit, especially when the circuit is old and therefore wears out. Intermittent errors are occasional error bursts that usually repeat themselves every now and then, i.e. are not continuous as permanent errors. These errors are caused by unstable or marginal hardware, and are activated by environmental changes such as temperature or supply voltage change. Transient errors are temporal single malfunctions caused by temporary environmental conditions which can be external phenomenon such as radiation or noise originating from the other parts of the chip.

Sources of errors can be classified according to the phenomenon causing the error. Such origins are for instance: the manufacturing process, physical changes during operation, internal noise caused by other parts of the circuit and external noise originating from the chip environment.

SINGLE ELECTRON TRANSISTORS

The end of the ITRS roadmap for classical CMOS devices and circuits envisions the emergence of future nanotechnologies and nano-devices, and also evidences many new related challenges. Logic design at present is solely applied to microelectronics. The process of transferring circuits and systems to nanoelectronics and relevant hybrid technologies (e.g., molecular electronics) has already started. Very fundamental and technological differences between nanoelectronic devices and microelectronic devices exist, those latter possibly in the nanometer size domain. Even though CMOS devices are reaching below 50nm dimensions, these devices rely on enhanced but standard CMOS fabrication processes, and hence do not formally participate to nanoelectronic devices. Novel physics, integrated with design methods and nanotechnology, leads to far-reaching revolutionary progress. One of the devices that