Chapter 4
Hardware Virtualization on Dynamically Reconfigurable Processors

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ABSTRACT
Numerous research efforts in reconfigurable embedded processors have shown that augmenting a CPU core with a coarse-grained reconfigurable array for application-specific hardware acceleration can greatly increase performance and energy-efficiency. The traditional execution model for such reconfigurable co-processors however requires the accelerated function to fit onto the reconfigurable array as a whole, which restricts the applicability to rather small functions. In the authors' research presented in this chapter, the authors have studied hardware virtualization approaches that overcome this restriction by leveraging dynamic reconfiguration. They present two different hardware virtualization methods, virtualized execution and temporal partitioning, and introduce the Zippy reconfigurable processor architecture that has been designed with specific hardware virtualization support. Further, the authors outline the corresponding hardware and software tool flows. Finally, the authors demonstrate the potential provided by hardware virtualization with two case studies and discuss directions for future research.

INTRODUCTION
In this chapter, we present results from the Zippy research project (Plessl, 2006, Plessl, Platzner, & Thiele, 2006, Enzler, Plessl, & Platzner, 2005, Plessl & Platzner, 2005, Enzler, Plessl, & Platzner, 2003b, 2003a, Enzler, 2004) that was started at ETH Zurich in 2001 and was continued later at University of Paderborn. At the center of the Zippy project stands the novel Zippy reconfigurable processor architecture, which comprises an embedded CPU core and an attached coarse-grained multi-context reconfigurable array. Zippy has been
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designed to support rapid dynamic reconfiguration at runtime as the prime feature of the architecture. The key objective of the Zippy research effort is to identify the potential of rapid reconfiguration in an embedded computing context. In particular, we have studied hardware virtualization as one particularly interesting application domain for dynamic reconfiguration which allows for exploring new performance versus chip-size versus energy trade-offs in the architecture design phase. For increasing the efficiency of hardware virtualization, we have augmented the Zippy architecture with specific hardware components that implement the execution models required for hardware virtualization directly in hardware.

This chapter is structured as follows. In Section Background we present an overview of the area of reconfigurable processors. We present related work and discuss the motivation and need for hardware virtualization as a new approach to balance performance, energy efficiency and chip size in embedded processors. We introduce two hardware virtualization approaches denoted as virtualized execution and temporal partitioning that we have explored in our work. In Section Zippy Dynamically Reconfigurable Processor Architecture we present the architecture of the Zippy reconfigurable processor and point out the dedicated hardware units for efficient hardware virtualization. In Section Tool Flows we briefly introduce the hardware tool flow for mapping hardware accelerators to the reconfigurable array and the compilation tool chain. Section System-Level Cycle-Accurate Co-Simulation introduces our system-level co-simulation environment that allows us to accurately evaluate a broad variety of reconfigurable processor architectures. In Section System-Level Cycle-Accurate Co-Simulation we explain how the hardware virtualization techniques outlined in Section Background are supported by the Zippy architecture and we present two detailed case studies that demonstrate and evaluate the benefits of hardware virtualization on our architecture. Finally, we present an outlook on future trends in Section Future Trends and summarize the conclusions from our work in Section Conclusions.

BACKGROUND

The design and implementation of embedded systems is generally challenging due to the stringent performance, power and cost constraints. It has been shown for many applications that co-processors based on field-programmable reconfigurable hardware devices, such as FPGAs, allow for significant speedups, cost and energy savings over embedded systems based on general-purpose microprocessors or microcontrollers. However, mapping complete applications rather than kernels to a reconfigurable device is difficult and often inefficient. It is useful to offload the performance hungry and latency sensitive application kernels to a reconfigurable coprocessor, while relying on a comparatively simple CPU core for handling the system management and control tasks that are not performance critical. Hence a processor architecture that combines reconfigurable hardware with a general-purpose CPU core in an integrated device is an attractive platform for building embedded systems. These architectures, denoted as reconfigurable processors have received increasing attention in the last years and a number of architectures have been introduced both in academic research and in the commercial marketplace.

Another trend that has emerged in recent years is the exploration of coarse-grained reconfigurable architectures. While fine-grained FPGAs are suitable for accelerating bit-oriented and custom operations, coarse-grained architectures operate on word-sized data and are particularly suitable for arithmetically intensive digital signal processing applications, as they occur in many embedded computing applications. Around the year 2000, a number of academic research projects have been started to study the potential of coarse-grained
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