Chapter 18

Flexible Implementation of Industrial Real-Time Servo Drive System

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ABSTRACT

The research presented in this chapter deals with the design and implementation of Real-Time (RT) control systems applying advanced Field Programmable Gate Array (FPGAs). The chapter proposes a promising flexible architecture that uses RT Operating System (RTOS) and ready-to-use Intellectual Properties (IPs). The authors detail an approach that uses software closed control loop function blocks (FB), running on embedded processor cores. These FBs implement the different control drive sub-modules into RTOS tasks of the execution environment, where each task has to be executed under well defined conditions. Two RTOSes are evaluated: µC-OS/II and Xilkernel. The FPGA embedded processor cores are combined with reconfigurable logic and dedicated resources on the FPGA. This System-on-Chip (SoC) has been applied to electric motors drive. A comparative analysis, in terms of speed and cost, is carried-out between various hardware/software FPGA-based architectures, in order to enhance flexibility without sacrificing performance and increasing cost. Case studies results validate successfully the feasibility and the efficiency of the flexible approach for new and more complex control algorithms. The performance and flexibility of FPGA-based motor controllers are enhanced with the reliability and modularity of the introduced RTOS support.

DOI: 10.4018/978-1-60960-086-0.ch018
INTRODUCTION

Nowadays, motor control researchers are increasingly developing new sophisticated control algorithms to increase performances and to optimize the efficiency of motors in a factory: i.e. sensorless control, neural network control, fuzzy logic control, Field Oriented Control (FOC), direct torque control, etc. These developments are always characterized by a growth of complexity. Indeed, the sophisticated control laws are constituted of heterogeneous functions because of the diversities in algorithm operations (memory storage, floating point arithmetic operations, trigonometric functions, integration, regulation, etc.) and differences in computation rate. Moreover, the control algorithms present always recursive computing that complicates the digital data coding. With this growing complexity of motor and motion control applications, there are larger computational requirements on the processor. The design challenge for embedded motors controlling machinery becomes how to integrate control complexities of high-sampling-frequency applications that can execute efficiently on limited resources and that meet not just higher performance but more flexibility as well. Many control applications require updated drive control algorithms and have to be changed and adjusted to their environment to reduce development costs.

So it becomes apparent that advanced Field Programmable Gate Array (FPGA), containing both reconfigurable logic blocks and embedded processor cores (Fletcher, 2005), offers significant advantages in the area of performance and flexibility. This Advanced FPGA technology (Rodriguez-Andina, Moure, & Valdes, 2007) becomes quite mature for high-speed power control applications (Ben Salem, Ben Othman, & Ben Saoud, 2008), since it has presented a good compromise between the programmable solution flexibility, and the efficiency and high-performance of a specific architecture. New FPGA capabilities have offered the means to create high-performance digital components allowing implementation of more complex control applications. But the key issue in a System-on-Chip (SoC) (Eshraghian, 2006; Nurmi, 2007) design is to trade-off efficiency against flexibility. Therefore, there are a lot of challenges regarding SoC design methodologies and architectures styles. Nowadays SoC designers face important product development decisions in choosing Intellectual Property (IP) cores for SoC. Indeed, determining which core is most appropriate for a given SoC requires careful consideration. Decisions must be made about the type of core (soft vs. hard), the architecture to integrate this core, and the relationships between HardWare (HW) and SoftWare (SW).

In advanced FPGA design (Jóźwiak, Nedjah, & Figueroa, 2010), System-on-Programmable Chip (SoPC) for motion control results in very complex tasks involving SW and HW skilled developers. Therefore, there is a need to a co-design expertise to build a powerful digital embedded controller. But, the power of FPGAs has been made readily available to embedded system designers and SW programmers through the use of high-level HW description tools (Vega-Rodríguez, Sánchez-Pérez, & Gómez-Pulido, 2005). These co-design tools help engineers to overcome the lack of expertise in digital HW design.

Moreover, the implementation of digital control systems and RT systems belong together and they should be connected in the design process, as a substantial percentage of control applications have either timing critical or high throughput requirements. Therefore, embedded Real-Time (RT) control becomes a promising research domain. Control systems are commonly designed using a set of cooperating periodic sub-modules that must be able to perform assigned calculations within demanding timing constraints, in order to ensure a correct dynamic behavior of the closed loop controller. To achieve this goal, the previous FPGA-based platforms advantages should be combined with the modularity and predictability
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