Chapter 14
Joint Validation of Application Models and Multi-Abstraction Network-on-Chip Platforms

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ABSTRACT
Application models are often disregarded during the design of multiprocessor Systems-on-Chip (MPSoC). This is due to the difficulties of capturing the application constraints and applying them to the design space exploration of the platform. In this article we propose an application modelling formalism that supports joint validation of application and platform models. To support designers on the trade-off analysis between accuracy, observability, and validation speed, we show that this approach can handle the successive refinement of platform models at multiple abstraction levels. A case study of the joint validation of a single application successively mapped onto three different platform models demonstrates the applicability of the presented approach.

INTRODUCTION
The design space of multiprocessor systems based on Network-on-Chip (NoC) interconnects is very large. Considering the interconnect structure alone, designers must choose or parameterise a large number of components according to application-specific constraints, such as buffering and flow control mechanism, network topology, word width, packet structure, or routing algorithm.

In this article, we propose a model-based methodology to evaluate the performance of a particular setup of a NoC interconnect under the constraints of a particular application. Our goal
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is to support the creation of a unified application model, which we can jointly validate with different platform models, each representing an alternative configuration of the NoC interconnect.

The validation of application models and platform models for NoC-based systems can be performed in several ways, ranging from formal and semi-formal approaches based on graph representations of both application and platform (Hu & Marculescu, 2005) to ad-hoc approaches that actually emulate the execution of the application on a prototype of the NoC using multiple FPGA boards (Saint-Jean et al., 2005). The next section presents further details of such approaches. Our approach combines semi-formal techniques with executable and simulatable models for joint validation of the application and platform. Both models are based on the principles of actor-orientation (Eker et al., 2003), which the Application Modelling Section covers. Actor-oriented models include the explicit description of the concurrent behaviour of the model’s components. To improve the expressiveness of actor-oriented models, we extend them by using Unified Modelling Language (UML) (Object Management Group, 2005) sequence diagrams for explicit ordering of inter-component communication. Applying such technique to application modelling is also addressed in the Application Modelling Section, whose particular emphasis is on the employment of hierarchical composition of systems with heterogeneous models of time and concurrency (one of the major benefits of actor-orientation). The Platform Modelling Section covers the modelling of hardware platforms based on NoCs. Within the scope of this article, a hardware platform includes the interconnect structures, an abstract representation of processing and storage elements, and a number of observability features (referred as scopes). We present a few strategies for the modelling of such platforms, each of them having different characteristics regarding simulation speed, accuracy, observability, and modelling effort. The Application Mapping onto Succes-

ively Refined Platform Models Section presents a methodology for the exploration of those different platforms in order to meet the application requirements. Furthermore, we present a case study of the validation of the proposed methodology. Then we analyse qualitatively each modelling strategy and comparatively the performance results obtained from different configurations of the NoC interconnect. Finally, we conclude the article and present some future work.

RELATED WORK

This article is based on the premise that it is necessary to consider the impact of the application on its underlying platform early at the design process in order to meet all performance, area, power consumption, and time-to-market constraints. Many research initiatives are also built on that premise, especially in multiprocessor System-on-Chip (MPSoC) design. Some of them are detailed below.

Kempf et al. (2006) present a framework targeted to MPSoC software development, verification, and evaluation. Their framework does not require the platform model to be complete before the software development can start. Software can be developed in four different levels of abstraction that vary in accuracy and simulation speed. The framework uses SystemC for simulation and XML to describe task mappings and timings. Furthermore, the framework provides an efficient design space exploration environment for instance by providing designers with various communication architectures. Ristau et al. (2008) discuss design space exploration early at the design process as well as the exploration of different mapping strategies. However, their application and platform models are simplified, disregarding the inter-process communication costs. Lei and Kumar (2003) describe the application as parameterisable task graphs, which are mapped onto NoC architecture. Their work aims at supporting mapping based on genetic algorithms.