Chapter 11

Self-Calibrating Source Synchronous Communication for Delay Variation Tolerant GALS Network-on-Chip Design

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ABSTRACT

Source synchronous links for use in multi-synchronous networks-on-chip (NoCs) are becoming the most vulnerable points for correct network operation and must be safeguarded against intra-link delay variations and signal misalignments. The intricacy of matching link net attributes during placement and routing and the growing role of process parameter variations in nanoscale silicon technologies are the root causes for this. This article addresses the challenge of designing a process variation and layout mismatch tolerant link for synchronizer-based GALS NoCs by implementing a self-calibration mechanism. A variation detector senses the variability-induced misalignment between data lines with themselves and with the transmitter clock routed with data in source synchronous links. A suitable delayed replica of the transmitter clock is then selected for safe sampling of misaligned data. The manuscript proves robustness of the link in isolation with respect to a detector-less link, but also assesses integration issues with the downstream synchronizer and switch architecture, proving the benefits in a realistic experimental setting for cost-effective NoCs.

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voltages and frequencies. In this context, multisynchronous designs, making use of synchronizers and source-synchronous communication for clock domain crossing, turn out to be a more flexible and readily available alternative to embody the GALS concept into industry-relevant designs rather than clockless handshaking.

In source synchronous links, data is routed together with a strobe signal (it might be the transmitter clock itself) which enables safe sampling at the receiver side regardless of the clock phase and/or frequency ratio between the communicating clock domains. However, synchronization interfaces now become the true weak-point of the system that needs to be safeguarded against timing failures. In fact, source synchronous links are generally designed under the assumption that there will be no or very limited routing skew between data lines and the transmitter clock, an assumption that might be easily impaired in nanoscale CMOS processes. The reason for this is twofold. On one hand, significant length, resistance, and load deviations among different wires of a link should be expected even when advanced bus routing features of place-and-route tools are used. On the other hand, process parameter variations impact various device characteristics, such as effective gate length, oxide thickness, and transistor threshold voltages, which may in turn lead to significant variations in power consumption and to timing violations. These effects impair the functionality of the link by reducing the data stability window and by causing the uncertainty on the precise sampling time over the clock period.

Although reducing delay variations between wires of a GALS NoC link would be the ideal requirement for advanced NoC implementation styles, it is virtually impossible to completely predict nominal delay and routing skew deviations occurring in the manufacturing process. Therefore, NoC link design should consider self-calibration, which is the approach taken by this manuscript. Instead of relying on the worst-case characterization of design parameters, self-calibrating systems determine autonomously the boundary of correct behavior, and set design parameters accordingly.

In this work we apply the self-calibration design principle to source synchronous links for use in synchronizer-based GALS NoCs. The basic idea is to use a variability detector at the receiver side of a source synchronous link with the capability of sensing the offset between data wires with each other and with the transmitter clock routed along with them. Based on misalignment quantification, the circuit selects the earliest delayed replica of the transmitter clock which can safely sample input data in the synchronization interface. The detector is meant for use during system reset, during which each GALS link is supposed to perform a self-calibration procedure. Repeated at every system bootstrap, the procedure can ensure robustness against wear-out effects.

**RELATED WORK**

Many recent works analyze the impact of process variations on the performance of integrated circuits, providing data on how parameter variations impact the maximum design frequency (Bowman et al., 2002) or variability models that characterize variations in microarchitecture (Sarangi et al., 2008; Bonesi et al., 2008). However, these studies do not consider the implications of variations in the interconnect infrastructure. Although (Nicopoulos et al., 2010) is a step forward in this direction, this study neglects the impact of manufacturing deviations on NoC links. Unfortunately, this impact is not negligible (Mondal et al., 2007; Hernández et al., 2010; Hassan et al., 2009). On one hand, although there are examples of repeater-less NoC self-calibrating links (Jose et al., 2005), they typically undergo repeater insertion. Therefore, they suffer from Lgate variations and dopant fluctuations in the transistors building up repeater stages, and also suffer from the variability introduced by the chemical metal planarization process (Mondal et al., 2007).
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