Event Report:
International Symposium on System-on-Chip 2012

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International Symposium on System-on-Chip 2012 was the 14th SoC event in Tampere, Finland. This paper discusses briefly the history of the event which is technically co-sponsored by IEEE Circuits and Systems Society. The main focus is in an overview of the year 2012 contents, and in particular in its invited talks.

INTRODUCTION

The history of the International Symposium on System-on-Chip dates back to 1999 when the first SoC event was organized in Tampere, Finland. It contained from the beginning almost all the elements that are characteristic to it nowadays. The event is based on a balanced mixture of

- World-class invited presentations;
- Exhibition of state-of-the-art commercial technology;
- Contributed paper track (since 2003);
- Industrial paper track;
- Panel discussion;
- Full-day tutorial (since 2001).

The first few events were built around a lot of invited talks by distinguished academics, people from leading companies, and from interesting start-ups in the emerging field of System-on-Chip. The industrial presentations, exhibits and a panel on timely topics in the field also have been there from day one. In 2003, SoC was turned to a full-fledged conference with also papers contributed by scientist in the field. At the same time, technical co-sponsorship was acquired from the Circuits and Systems Society of IEEE. Since that, the peer-reviewed papers have also been published in the proceedings and in IEEE Xplore database.

The mission of SoC is to provide a forum that is fully and comprehensively dedicated to SoC issues. It was the first annual event worldwide to use exclusively “SoC” in its name. Traditionally, it is the place where the academy and industry keep meeting each others. This is reflected also in the participation and sponsorship by local industry, e.g., in 2012 Nokia was the main financial sponsor. SoC has been organized by Tampere University of Technology (TUT), Department of Computer Systems. For the coming years this will change, as the main organizing group has been merged to the
Nevertheless, the organization will continue and the location will keep being anchored to Tampere – The SoC City (SoC, 2012). The rest of the paper will give an overview of SoC 2012.

**SOC 2012**

The International Symposium on System-on-Chip 2012 was bearing a special theme on Reconfigurable Circuits and Systems. The event was organized by TUT, Department of Computer Systems on October 11-12. The participants of the conference were representing about 15 different nationalities. The event was co-located with the Embedded Systems Week taking place October 7-12 2012. Both took place in Tampere Hall, the largest conference center in Nordic countries (see Figure 1).

**Invited Talks Addressed Reconfigurable Circuits and Systems**

On Thursday, two invited speakers were on stage. In his speech, Emmanuel Casseau from the University of Rennes1, France, discussed ROMA, a Reconfigurable Operator Based Architecture for Multimedia Applications. In multimedia applications, video and image processing is one of the challenges embedded systems have to face. Such applications are typically computationally intensive with control statements, and designers have to cope with stringent requirements on power and performance. The ROMA project proposes to develop both a design methodology and a reconfigurable processor able to adapt its computing structure to video and image processing applications. The reconfigurable processor is in charge of implementing parts of the code corresponding to loops and frequently executed computation code fragments that can be accelerated and/or which are good candidates to save power. It is built around a pipeline of coarse grain reconfigurable operators exhibiting interesting performance/power trade-off. The operators are designed such that their granularity matches the domain-specific computation patterns. Flexibility is obtained through these operators which can be configured for the function they implement and the width of the data. There is also a design flow to configure the processor. From the application source code, the software framework identifies the different computation

*Figure 1. Tampere Hall*
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