Cluster Based Networks-on-Chip: An Efficient and Fault-Tolerant Architecture using Network Interface Assisted Routing

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ABSTRACT

Partial Virtual channel Sharing (PVS) architecture has been proposed to enhance the performance of Networks-on-Chip (NoC) based systems. In this paper, the authors present an efficient and reliable Network Interface (NI) assisted routing strategy for NoC using PVS architecture. For this purpose, NoC system is divided into clusters. Each cluster is a group of two nodes comprising Processing Elements (PE), switches, links, etc. Each PE in a cluster can inject data to the network through a router, which is closer to the destination. This helps to reduce the network load by reducing the average hop count of the network. The proposed architecture can recover the PE disconnected from the network due to network level faults by allowing the PE to transmit and receive the packets through the other router in the cluster. 5×6 crossbar is used for the proposed architecture which requires one more 5×1 multiplexer without increasing the critical path delay of the router as compared to the 5×5 crossbar. The proposed router has been simulated for uniform, transpose and negative exponential distribution (NED) traffic patterns. The simulation results show the significant reduction in average packet latency at the expense of negligible area overhead.

Keywords: Fault Tolerance, Network Interface (NI), Networks-on-Chip (NoC), Resource Utilization, Virtual Channel Sharing

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1. INTRODUCTION

Networks-on-Chip (NoC) has been proposed for System-on-Chip (SoC) based applications to achieve the better performance with lower power consumption as compared with typical on-chip bus architectures (Jantsch & Tenhunen, 2003). A typical NoC based system consists of processing elements (PE), network interfaces (NI), routers and channels. The router further contains switch, buffers and routing logic as shown in Figure 1. All links in NoC can be simultaneously used for data transmission, which provides a high level of parallelism. It is an attractive solution to replace the conventional communication architectures such as shared buses or point-to-point dedicated links by NoC.

Buffers consume the largest fraction of dynamic and leakage power of the NoC node (router + link; Banerjee, Vellanki, & Chatha, 2004). Storing a packet in buffer consumes far more power as compared to its transmission (Ye, Benini, & De Micheli, 2002). Thus, increasing the utilization of buffers and reduction in their number and size with efficient autonomic control reduces the area and power consumption. Wormhole flow control (William J. Dally, 2004) has been proposed to reduce the buffer requirements and enhance the system throughput. However, one packet may occupy several intermediate switches at the same time. This introduces the problem of deadlocks and live locks (Luca Benini, 2006). To avoid this problem the use of virtual channel is introduced. Virtual channel flow control exploits an array of buffers at each input port. By allocating different packets to each of these buffers, flits from multiple packets may be sent in an inter-

Figure 1. Conventional virtual channel NoC router architecture
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