This special issue of IJERTCS continues with the System-on-Chip theme of the previous issue with two articles and a conference report. The last article of this issue extends the coverage to location aware routing over asymmetric links. For the System-on-Chip theme, we express our warmest gratitude to the guest reviewers of the articles, for their valuable comments and suggestions to further improve the manuscripts.

System-on-Chip accumulates all the design challenges of energy-efficient microelectronics circuits, powerful computing elements, timely and reliable communication infrastructure, real-time software, and intelligent complex embedded systems. This all must be addressed in a short time to get the low-cost products out on the market in the short profitable time window of the contemporary consumer markets.

The trend of ever-decreasing feature size in the silicon manufacturing process poses electrical challenges, such as cross-talk, power droops, thermal effects, and leakage currents. Powerful computing elements range from hardwired functions to reconfigurable architectures, and naturally also software-programmable processors which may be general-purpose, or – in the quest for combining energy-efficiency and powerful operation – built specifically to the application at hand.

Increasingly the multi-core and many-core approaches are conquering the SoC era, too, where they are called Multi-Processor System-on-Chip (MPSoC). This further complicates the software design for SoC, and also emphasizes the role of high-throughput on-chip interconnects. The trend there is towards Network-on-Chip communication architectures, borrowing some key principles from macro scale computer networks and telecommunication infrastructure.

System design, whether on-chip or in larger contexts, requires good methodologies and tools. Tooling is also a key issue on many levels of SoC design and deployment, from system modeling and design, software compilation and architectural design down to the design and test of nanoscale integrated circuits. The use of abstraction and powerful design languages is a key element in the specification, design and verification of SoCs. The bottomline are the SoC applications, which add many interesting flavors to the field with their own specific constraints in terms of cost, energy, reliability, and complexity.

The first two articles of this issue are some of the most interesting topics from the SoC symposium that were selected for inclusion in the journal after extension and enhancements. The SoC topics range from design tools and methodology through system architecture and demanding applications down to manufacturing technology related electrical properties.
2010 was the 12th annual SoC event in Tampere, Finland. At the end of this issue there is a conference report on the event. SoC is devoted to all aspects of System-on-Chip, and in 2010 particularly to MPSoC-related issues.

The multiprocessor SoCs are largely relying on networked interconnects. In the first article, *Self-Calibrating Source Synchronous Communication for Delay Variation Tolerant GALS Network-on-Chip Design*, written by researchers for the University of Ferrara, Italy, and Technical University of Valencia, Spain, the authors are addressing the vulnerability of source synchronous links in Networks-on-Chip (NoC). In particular, they are discussing the challenge of designing a process variation and layout mismatch tolerant link for synchronizer-based GloallyAsyncronous, Locally Synchronous (GALS) NoCs by implementing a self-calibration mechanism. They present a variation detector which guarantees the reliability of NoC source synchronous interfaces under high variability. The variability detector is placed in front of the regular synchronizers in the communication architecture. They consider different cases of mismatch: misalignment between data and clock, misalignment between wires of the data link, and even random process variability of the detector’s own logic cells. Analysis of the comprehensive metric of skew tolerance for a mesochronous synchronizer has revealed that the insertion of the variation detector has advantages in most cases and for the main synchronization architectures of practical interest (loosely vs. tightly coupled with the NoC). Even for non-variability-dominated links, the architecture with a variability detector can better cope with the layout constraints of the link.

In the second article, *Checkpointing SystemC-Based Virtual Platforms*, written by the researchers from RWTH Aachen University and Synopsys Inc., Aachen, Germany, the target is to introduce checkpointing to virtual platform simulations, enabling to restore a virtual platform from a previously saved simulation state. Virtual platforms are executable software models of hardware systems, particularly useful for starting the software development in an early design phase when the computing hardware is not yet available. Checkpointing can considerably shorten the edit-compile-debug cycle for software developers in such cases. For a practically useful checkpoint/restore technique, a number of issues have to be taken into account, including reliability, transparency, performance, support for external applications such as graphical user interfaces and debuggers, and support for operating system (OS) resources. The authors present a novel checkpoint framework for virtual platforms, based on user level process checkpointing. The framework for handling external communication channels and OS resources during the checkpoint and restore procedure allows the integration of user modules, debuggers and GUIs. The user-defined modules are notified about checkpoint and restore events by inheriting from a special observer object. All the OS resources and external connections have to be released in order to store the status of the platform in a safe and restorable state. The performance was evaluated using an ARM-based platform. In order to mitigate the large checkpoint size, the checkpoints can be compressed before being stored. On average a compression of 10x is reached.

The last article of this issue, written by Mitra and Poellabauer from University of Notre Dame, USA, was peer-reviewed by members of the IJERTCS editorial board during spring 2011. The article, *Asymmetric Geographic Forwarding: Exploiting Link Asymmetry in Location Aware Routing*, introduces a location aware routing approach called A-GF (asymmetric geographic forwarding). The approach takes advantage of asymmetric links in increasing the reliability and performance of ad-hoc routing. Link asymmetry in wireless transmission occurs when the transmission ranges of communicating parties are asymmetric: the station with a wider transmission range is able to successfully reach its peer station, but the peer station’s transmission range is not wide enough to reach the other station. In this situation, only one-way transmissions are possible. Existing geographic forwarding algorithms assume that their environment consists of symmetric links.
By discovering and exploiting also the asymmetric links the routing hop count is reduced, latencies decrease and routing reliability is improved. In making routing decisions, A-GF uses stability and minimum latency as metrics. The results of the work encourage the authors to further investigate the possibilities of combining stability and energy efficiency in asymmetric wireless transmission as their future work.

We thank all the contributors and reviewers of this issue of IJERTCS, and wish all readers an enlightening reading experience with the research articles published in this issue.

Jari Nurmi
Guest Editor
Seppo Virtanen
Editor-in-Chief
IJERTCS

Jari Nurmi is a professor of Computer Systems at Tampere University of Technology (TUT). He has held various research, education and management positions at TUT and in the industry since 1987. He got a PhD degree from TUT in 1994. His current research interests include System-on-Chip integration, embedded and application-specific processor, multiprocessor and reconfigurable architectures, and circuit implementations of positioning, DSP and digital communication systems (including Software-Defined Radio approach). He is leading a group of about 20 researchers. Dr. Nurmi is the general chairman of the annual International Symposium on System-on-Chip (SoC) and its predecessor SoC Seminar in Tampere since 1999, and a board member of ICL-GNSS, SoC, FPL, and NORCHIP conference series. He was/is also the general chair of FPL 2005, SiPS 2009, ICL-GNSS 2011, DASIP 2011 conferences. He was the head of the national TELESOC graduate school 2001-2005. He is the author or co-author of about 250 international papers, editor of Springer book "Processor Design: System-on-Chip Computing for ASICs and FPGAs," co-editor of Kluwer book "Interconnect-centric Design for Advanced SoC and NoC", associate editor of the "International Journal of Embedded and Real-Time Communication Systems," and is now editing Springer books on “GALILEO Positioning Technology” and “Computation Platforms for SDR.” He has supervised 110 MSc theses and 12 Doctoral theses at TUT, and been the opponent or reviewer of 15 PhD theses in other universities. He is a senior member in IEEE Circuits and Systems Society, Computer Society, Signal Processing Society, Solid-State Circuits Society and Communications Society. In 2004, he was one of the recipients of Nokia Educational Award, and the recipient of Tampere Congress Award 2005. He was awarded one of the Academy of Finland Research Fellow grants for 2007-2008. He is also reviewing projects for EU and project proposals for national funding agencies in Belgium, Canada, The Netherlands, Saudi-Arabia, Slovenia, Sweden, and Switzerland.

Seppo Virtanen received his BSc in applied physics, MSc in electronics and information technology (1998), and DSc (Tech.) in communication systems (2004) from the University of Turku (Finland). Since 2009 he has been adjunct professor of embedded communication systems at the University of Turku. He is a Senior Member of the IEEE. His research interests include the design and methodological aspects of reliable and secure systems.