Guest Editorial Preface

Special Theme Issue on System-on-Chip

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To start with, I would like to thank Editor-in-Chief Seppo Virtanen for the opportunity to assemble this special issue. The cooperation was once again very smooth. I express my warmest gratitude also to the reviewers of the extended papers, for their valuable comments and suggestions to further improve the manuscripts.

System-on-Chip accumulates all the design challenges of energy-efficient microelectronics circuits, powerful computing elements, timely and reliable communication infrastructure, real-time software, and intelligent complex embedded systems. This all must be addressed in a short time to get the low-cost products out on the market in the short profitable time window of the contemporary consumer markets.

The trend of ever-decreasing feature size in the silicon manufacturing process poses electrical challenges, such as cross-talk, power droops, thermal effects, and leakage currents. Powerful computing elements range from hardwired functions to reconfigurable architectures, and naturally also software-programmable processors which may be general-purpose, or – in the quest for combining energy-efficiency and powerful operation – built specifically to the application at hand.

Increasingly the multi-core and many-core approaches are conquering the SoC era, too, where they are called Multi-Processor System-on-Chip (MPSoC). This further complicates the software design for SoC, and also emphasizes the role of high-throughput on-chip interconnects. The trend there is towards Network-on-Chip communication architectures, borrowing some key principles from macro scale computer networks and telecommunication infrastructure.

System design, whether on-chip or in larger contexts, requires good methodologies and tools. Tooling is also a key issue on many levels of SoC design and deployment, from system modeling and design, software compilation and architectural design down to the design and test of nanoscale integrated circuits. The use of abstraction and powerful design languages is a key element in the specification, design and verification of SoCs. The bottom line are the SoC applications, which add many interesting flavors to the field with their own specific constraints in terms of cost, energy, reliability, and complexity.

International Symposium on System-on-Chip 2012 was the 14th annual SoC event in Tampere, Finland. This special issue consists of

some of the most interesting papers that were selected for inclusion in the journal after some extension and suggested enhancements. At the end of this issue there is also a conference report on the SoC event. SoC is devoted to all aspects of System-on-Chip, and in 2012 particularly to reconfigurable circuits and systems.

Dataflow modeling offers a myriad of tools to improve optimization and analysis of signal processing applications, and is often used by designers to help design, implement, and maintain Systems-on-Chip for signal processing. However, maintaining and upgrading legacy systems that were not originally designed using dataflow methods can be challenging. The researchers from University of Maryland tackle this issue in their paper "Instrumentation-Driven Model Detection and Actor Partitioning for Dataflow Graphs." Designers often need convert legacy code to dataflow graphs by hand, which can be very difficult and time consuming. In their paper, the authors develop a method to facilitate this conversion process by automatically detecting the dataflow models of the core functions from bodies of legacy code. They focus first on detecting static dataflow models, such as homogeneous and synchronous dataflow, and then present an extension that can also detect dynamic dataflow models. Building on their algorithms for dataflow model detection, they present an iterative actor partitioning process that can be used to partition complex actors into simpler sub-functions that are more prone to analysis techniques.

Further down the design flow, the application has to be mapped on the implementation platform. The efficient analysis and exploration of mapping solutions of a parallel application on a heterogeneous Multi-Processor System-on-Chip (MPSoC) is usually a challenging task in system-level design, in particular when the architecture integrates hardware cores that may expose reconfigurable features. The paper of researchers from Politecnico di Milano, titled "A Simulation-based Framework for the Exploration of Mapping Solutions on Heterogeneous MPSoCs," addresses this issue. The paper proposes a system-level design framework based on SystemC simulations for fulfilling this task, featuring an automated flow for the generation of timing models for the hardware cores starting from the application source code, an enhanced simulation environment for SystemC architectures enabling the specification and modification of mapping choices only by changing an XML descriptor, and also a flexible controller of the simulation environment supporting the exploration of various mapping solutions featuring a customizable engine. The proposed framework has been validated with a case study considering an image processing application to show the possibility to automatically exploring alternative solutions onto a reconfigurable MPSoC platform.

There exist various implementation platforms optimized for different application domains. Wireless mobile terminal design is one delicate field calling for efficient realizations of multiple communications standards, sometimes even concurrently. In current era of complex chip designs targeting wireless mobile terminals, architects and designers need to conform to tight design constraints – both in terms of performance (e.g. execution time, silicon area, energy consumption) and time-to-market. The researchers from IMEC describe their solution to meet these challenging goals in their paper "Design Flow for Silicon Chip Implementing Novel Platform Architecture for Wireless Communication." They introduce a platform architecture that uses a decentralized control to minimize communication and control overhead while keeping timing predictable by using state-of-the-art components and a novel interconnect. They demonstrate three main achievements in running multiple wireless standards on our platform: 1.053Gbps 4x4 80MHz WLAN 802.11ac receiver data path meeting the SIFS timing with a latency of 12.5µs, dual concurrent 173Mbps 2x2 20MHz Cat-4 3GPP-LTE receiver and platform reconfiguration from WLAN 11n receiver to 3GPP-LTE one in 52µs. They also describe the design flow used to prepare the main components of the platform architecture for a tape-out, while especially keeping a close eye on energy consumption. The chip design flow is rather generic and could be used in other custom processor chip designs even outside wireless domain.

When finally reaching the operational MPSoC application running on a number of cores, synchronization plays a key role in maintaining the correctness of the system functionality. Spinlocks are a common technique in Multi-Processor Systems-on-Chip (MPSoCs) to protect shared resources and prevent data corruption. Without a priori application knowledge, the control of spinlocks is often highly random which can degrade the system performance significantly. The researchers of RWTH Aachen and Synopsys present their work to this end in their article "Efficient Implementation of Application-Aware Spinlock Control in MPSoCs." To improve the synchronization performance, a centralized control mechanism for spinlocks is proposed in their paper, utilizing application-specific information during spinlock control. The complete control flow is presented, which starts from integrating high-level user-defined information down to a low-level realization of the control. An Application-Specific Instruction-set Processor (ASIP) called OSIP, which was originally designed for task scheduling and mapping, is extended to support this mechanism. The case studies presented demonstrate the high efficiency of the proposed approach and at the same time highlight the efficiency and flexibility advantages of using an ASIP as the system controller in MPSoCs.

These papers are samples on some of the most interesting aspects dealt with in the Symposium, which range from design tools and methodology through system architecture and demanding applications down to managing manufacturing technology related issues. At the end of this issue, there is a more comprehensive report on the event. Hoping to see you in Tampere – The SoC City – in the coming years.

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Jari Nurmi is a professor of Computer Systems at the Department of Electronics and Communications Engineering of Tampere University of Technology (TUT). He has held various research, education and management positions at TUT and in the industry since 1987. He got MSc and PhD degrees from TUT in 1988 and 1994, respectively. His current research interests include System-on-Chip integration, embedded and application-specific processor, multiprocessor and reconfigurable architectures, and circuit implementations of positioning, DSP and digital communication systems (including Software-Defined Radio approach). He is leading a group of about 15 researchers. Dr. Nurmi is the general chairman of the annual International Symposium on System-on-Chip (SoC) and its predecessor SoC Seminar in Tampere since 1999, and a board member of ICL-GNSS, SoC, FPL, DASIP and NORCHIP conference series. He was/is also the general chair of FPL 2005, SiPS 2009, ICL-GNSS 2011, DASIP 2011 conferences, the local organizer for ESWEEK 2012, and host of FPGAworld 2012 Tampere. He was the head of the national TELESOC graduate school 2001-2005. He is the author or co-author of well over 270 international papers, editor of Springer book Processor Design: System-on-Chip Computing for ASICs and FPGAs, co-editor of Kluwer book Interconnect-centric Design for Advanced SoC and NoC, associate editor of the International Journal of Embedded and Real-Time Communication Systems, and is now editing two more Springer books. He has supervised 119 MSc theses and 16 Doctoral theses at TUT, and been the opponent or reviewer of 20 PhD theses in other universities worldwide. He is a senior member in IEEE Circuits and Systems Society, Computer Society, Signal Processing Society, Solid-State Circuits Society and Communications Society. In 2004, he was one of the recipients of Nokia Educational Award, and the recipient of Tampere Congress Award 2005. He was awarded one of the Academy of Finland Research Fellow grants for 2007-2008, and in 2011 he was a co-recipient of IIDA Innovation Award. He is a member of IEEE CASS technical committee on VLSI Systems and Applications, and the board of Tampere Convention Bureau. He is also reviewing projects for EU and project proposals for national funding agencies in Belgium, Canada, The Netherlands, Saudi-Arabia, Slovenia, Sweden, and Switzerland.