EDITORIAL PREFACE

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The contemporary trends in the ways we communicate today are rapidly developing an all-inclusive convergence of all media into one terminal. We can see users requiring wireless communication with universal and always-accessible internet availability. We can see users having a desire for uniform terminal equipment for most, if not all, communication types, incorporating reasonable size, battery-enabled mobility and substantial standby time. A hand-held mobile communication device is not anymore a telephone in the traditional sense; it is now a small embedded computer optimized for the different types of communication the user wishes to regularly engage in. Modern telephones, that is, smartphones, are nowadays used as personal calendars, game consoles, remote controls, music players, social media terminals, e-mail and web clients, and even televisions in addition to their original historical usage scenario of placing and receiving phone calls. The convergence is not necessarily leading to a situation where a specific type of communication is taken completely away from its traditional environment, but more to providing an adequate way of using a variety of communication applications in one device. It is still often users' preference to watch television broadcasts and movies on a large TV screen rather than on a smaller smartphone screen, but the ability to watch the news broadcast on-demand on a smartphone while on the move is a definite desirable added value to traditional telephony. Similarly, a television user may want the ability to make video calls and browse web pages using the television set while preferring to make video calls using a smart phone and to browse the web using a computer.

The converging development is made possible only through the active research performed in the field of embedded and real time communication systems. The disciplines of computer science, computer engineering, telecommunication and communication engineering are well established and scientists, researchers and industry professionals in these disciplines are numerous in all continents. The convergence of these disciplines into embedded and real-time communication systems is a natural development as can be seen for example in the smartphone and tablet industries today. The field is interdisciplinary in scope, binding together research from the mentioned disciplines with focus on how they converge to embedded and real-time systems for the communication application domain. In embedded and real-time communication systems, the system-level design process and the design of hardware and

software components of the system are facing brand new challenges: despite the small size and reliance on battery power, the devices need to be able to perform ever more complex operations and tasks while maintaining a low enough pricing scheme to ensure adequate market interest. The manufacturers and their design teams are therefore constantly forced to find a balance between adequate performance of the device (the device may not be too slow but it should not provide excess processing performance beyond its application range), low enough manufacturing and design costs and a short time-to-market.

Forthcoming research in embedded and real-time communication systems needs to target the challenges in future complex converged wireless systems by adventurous development and technological exploration, and experimentation with novel technologies, systems and system design methodologies. Key research areas in this respect are embedded system design, communication system design, system-wide security and hardware/software co-design, producing results that converge into novel technologies usable in future secure embedded communication systems.

This issue of *International Journal of Embedded and Real-Time Communication Systems* (IJERTCS) approaches the challenges described above with four research articles that have been received and peer-reviewed during 2012 and 2013. The first three articles focus on providing solutions for the complexity and power consumption challenges met in embedded and real-time system design today from the device design point of view. The fourth article takes a more high abstraction level approach for modeling and evaluating such hardware and software systems rapidly and efficiently.

In the first article of this issue, Subayal Khan, Jukka Saastamoinen, Jyrki Huusko and Juha-Pekka Soininen from VTT Technical Research Center of Finland and Jari Nurmi from Tampere University of Technology, Finland, the authors present a novel run-time statistics based application workload model extraction and platform configuration technique. In modern complex embedded communication system platforms it is necessary to support a variety of communication applications. For this purpose, the systems are required to contain multi-core processors, hardware accelerators and Intellectual Property (IP) cores integrated into a single integrated circuit (chip). The high complexity of both the platforms and the applications makes the design space very complex with a vast abundance of design alternatives. The system designer is required to quickly evaluate the performance of different application architectures and implementations on potential platforms. One of the most popular techniques employed nowadays is *system-level-performance evaluation* and it takes advantage of abstract workload and platform capacity models at a high abstraction-level, making model instantiation with reduced modeling effort higher simulation speeds possible. The novel technique presented by the authors is applicable to both distributed and non-distributed applications. The experimental results from two case studies show that the control of the workload models exactly mimics the way different functionalities are triggered during the application execution.

The second article, written by Renu Verma from Rama Institute of Technology, Kanpur, India, Mohammad Ayoub Khan from Centre for Development of Advanced Computing, Noida, India and Amit Zinzuwadiya from Amdocs, Haryana, India, investigates an important problem in irregular mesh Network-on-Chip (NoC) topologies. The authors propose an efficient deadlock-free routing algorithm for irregular mesh NoCs that significantly reduces the latency and power consumption of the system. The authors also point out the problems in the existing degree priority based routing algorithm. Finally, the authors propose an extended Logic Based Distributed Routing (LBDRe) method to remove deadlock situations without using a virtual channel in the degree priority based routing algorithm. According to the presented experimental results, the proposed routing algorithm reduces power consumption by 9–22% and overall average latency by 8–12%

with minimal hardware cost in comparison to previously presented solutions for irregular mesh NoC topologies.

In the third article, the authors Yul Chu and Marven Calagos from University of Texas Pan American, USA present a buffered dual-mode-access memory cache scheme to reduce power consumption for high associative caches in modern embedded systems, consisting of a most-recently-used (MRU) buffer table and a single cache structure to implement two access modes. A current trend in microprocessor design is to implement more high-tech functions using large caches. This may lead to increased power consumption which is very problematic for battery-powered mobile devices. Clearly there is a need for a low-power cache design that does not excessively trade off system performance. Based on the experimental results, the authors conclude that the proposed cache scheme reduces the power consumption significantly both for instruction and data cache use in comparison to existing approaches.

The fourth article is written by Djamel Eddine Saïdouni, Nabil Belala, Radja Boukharrou, Ahmed Chaouki Chaouche, Adel Seraoui and Asma Chachoua from Department of Computer Science and its Application, University Constantine 2, Algeria. The authors introduce an extension of Petri Nets called Time Petri Nets with Action Duration (DTPN), associating time with transitions. In the proposed approach, the firing of transitions is bound to a time interval and transitions represent actions which have explicit durations. The authors define operational semantics for DTPN using Durational Action Timed Automata (DATA). The DTPN approach presented in the article takes into account both timing constraints and durations under true-concurrency semantics, aiming at better expressing concurrent and parallel behaviors of real-time systems.

As a journal in the focal point of computer science, computer engineering, telecommunication and communication engineering, the *International Journal of Embedded and Real-Time Communication Systems* (IJERTCS) is positioned well to provide its readership with interesting and well-focused articles based on recent high-quality research. The journal's coverage in topics from embedded systems, real-time systems, and communication system engineering, and especially how these disciplines interact in the field of embedded and real-time systems for communication, offer its readership both theoretical and practical research facilitating the convergence of embedded systems, real-time computing, and communication system technologies and paradigms. IJERTCS is aimed to benefit scientists, researchers, industry professionals, educators and junior researchers like PhD students in the embedded systems and communication systems sector. The journal aims to provide its target audience with a forum to disseminate and obtain information on the most recent advances in embedded and real-time communication systems research: to give the readers the opportunity to take advantage of the research presented in the journal in their scientific, industrial or educational purposes. IJERTCS publishes high-quality articles based on recent important advancements in its research area, and aims for a fast turn-around time for submitted manuscripts.

I wish to thank all the contributors of this issue of IJERTCS, and I wish all readers an enjoyable and enlightening reading experience with the peer-reviewed research articles published in this issue.

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Seppo Virtanen received his BSc in applied physics, MSc in electronics and information technology (1998), and DSc (Tech.) in communication systems (2004) from the University of Turku (Finland). Since 2009, he has been Adjunct Professor of Embedded Communication Systems at University of Turku. He is Editor-in-Chief of the International Journal of Embedded and Real-time Communication Systems *and a senior member of the IEEE. His published academic research has been in the areas of hardware acceleration for protocol processing, protocol processor architectures, and hardware/software codesign methodologies for embedded communication systems. In the past few years, his research interests have been focused on platforms capable of handling the processing of communication protocols, DSP routines, and software defined radio algorithms and applications in parallel on a parameterizable hardware platform, as well as information security related topics in the embedded systems domain.*