GUEST EDITORIAL PREFACE

Special Issue on Networked Embedded Systems

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In the last decade, technology has so constantly progressed that, almost without noticing, we are now able to make our past dream -ubiquitous, pervasive and smart environments- come true. Now that we can "sense the world" via the numerous embedded logical or physical sensors, it is the time to expose the true social impact of these technologies.

Networked Embedded Systems (NES) find their ways into an increasing diversity of domestic and societal applications. Smart houses, next-general transportation systems, wireless multimedia sensor networks, ICT-enabled health systems, etc., all contain certain forms of parallel or distributed embedded sensors, controllers or computers in general. Under resource limitation and time-to-market pressure, NES needs to be scalable in terms of physical overhead, energy efficiency and design effort. Scalability can also be considered from the application's point of view- to obtain deployment services for distributed applications regardless of the platform, and the platform's point of view- to provide mechanisms for adding and removing any networked computational resources at run time. In addition to scalability, since processing, communication and control components may all potentially be integrated, research efforts are needed on the specification, modeling and characterization, partitioning, architecture and design flow for such heterogeneous computing platforms.

The special issue on Networked Embedded Systems in IJERTCS gathered four articles addressing different and complementing topics of networked embedded systems.

The first article of this issue "Reliability Modeling of Embedded Nodes in Real Time Wireless Systems" presents a framework to analyse how NES reliability is affected by the influence of the network dynamics or complex failure scenarios. NES modeling introduces new challenges when compared to traditional distributed systems analysis. Extra non-functional

dimensions (power consumption, real-time, mobility, etc.) get into the playground. This makes it quite difficult to perform fast and accurate system simulations at design time. Waiting to the deployment stages of the NES for finding out possible performance bottlenecks or infrastructure weakness is too costly.

One of the hot issues in this field is to obtain higher communication data rate where different efforts of communication standardization have been performed. In their paper "A Parallel Software Architecture for the LTE Protocol on a Multi-Core Mobile Modem", the authors from Duisburg, Germany describe novel software architecture and load balancing for the LTE protocol stack that allows concurrent execution on a multi-core processor and thus allows for exploiting all the advantages like higher performance through parallelism at low power consumption. Introducing parallel software architecture for the access stratum part of the LTE protocol stack on the mobile terminal, this work shows the benefits of using this architecture on multi-core mobile modem.

Security and privacy are important concerns for large-scale social applications, e.g. Facebook, Youtube or Flickr. The 3rd article "ECPDR: An Efficient Conditional Privacy-Preservation Scheme with Demand Response for Secure Ad hoc Social Communications" addresses this concern by proposing ECPDR scheme upon the ad-hoc social network model, based on a reactive routing protocol. The ECPDR scheme combines the efforts from certification, routing and handshaking techniques to detect and avoid harmful attacks on the content's security and privacy. The communication scheme is efficient in terms of transmission latency. We expect the extensive theoretical and quantitative evaluation (e.g. the attacks' detection rate and the communication performance) to be useful, in particular, to researchers working on wireless or mobile networks with security and privacy concerns.

The last article "A Reconfigurable Wireless Environment for ECG Monitoring and Encryption" provides a very practical case study for applying networked embedded systems (esp. the wireless sensor networks) to smart e-health environment. Out of a wide spectrum of related topics, authors focus on the implementation issues upon a reconfigurable (FPGA-based) platform. The architectural design centers around the implementation of AES (Advanced Encryption Standard) on FPGA hardwares, and demonstrates the proposed design is more efficient in terms of throughput than previous works. Most interestly, the authors have done a real demonstration with full coverage of sensing, encryption, decryption and display of ECG (electrocardiogram) data. Extensive quantitative analysis of performance and resource consumption is presented. This article provides useful insight on exploiting reconfigurable devices in implementing resource-limited, medium-scale ubiquitous embedded systems, e.g. personal area networks.

We thank all our anonymous reviewers and submitting authors in making this special issue. We hope that the diverse perspectives from the included articles will bring interesting insights to researchers, engineers and other professionals. For sure, we will observe new theories, architectures and techniques addressing the scalability, heterogeneity, security and privacy, as well as other advanced features on the rapidly developing NES technology in the near future.

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Julio Daniel Dondo Gazzano is an associate professor in the University of Castilla-La Mancha, Ciudad Real, Spain. He holds a Ph.D. degree from the same University, an M.Sc in Software Engineering and in Electrical/Electronic Engineering from the University of San Luis, Argentina. His research interests include the integration of complex embedded systems, dynamically reconfigurable computing, heterogeneous distributed systems and Reconfigurable Grid Computing. Dr Dondo Gazzano has served as PC members, session chairs in several conferences as JCE2012/13, EUROMICRO-DSD 2013. He has wide experience in the organization of several conferences, courses and events of scientific dissemination. He has participated as an author and co-author of more than 30 publications in international peer reviewed conferences and journals.

Jesús Barba received the MS and PhD degrees in Computer Engineering Diploma from the University of Castilla-La Mancha (UCLM), Spain, in 2001 and 2008 respectively. He is working as an Associate Professor with the Department of Information and Systems Technology (TSI) since 2001, lecturing in the area of Computer Architecture and Networks. He has also participated as part of the national quality mentioned Doctoral programme which is running in the TSI department, as an expert in the field of Heterogeneous Networked Systems. He is part of the ARCO research group, located at the School of Computer Science (UCLM, Spain) since 2000. In the beginning, he was involved in several projects related with advanced compilers for EPIC architectures and co-design of heterogeneous systems. Later on, Dr. Barba's research activity continued with CAD tools for HW/SW co-design and integration of reconfigurable systems. These two research lines converge in his PhD. dissertation where a system level heterogeneous middleware for reconfigurable embedded systems is proposed. Currently, his research interests comprise works in "Low cost, low power consumption reconfigurable systems for ubiquitous computing", "Reconfigurable computing platforms for AI algorithms", "Heterogeneous Distributed Embedded Computing" and "Design of embedded systems using High-level Synthesis Tools". Since 2012, he is overlapping his research activity with his position as a member of the Directive board at the School of Computer Science (UCLM, Spain) since 2012.

Liang Guang is a postdoctoral senior researcher in the laboratory of Embedded Computer and Electronic Systems at the Department of Information Technology, University of Turku, Finland. He holds a D.Sc. (PhD Tech.) degree from the same department, and a MBA certificate in innovation and growth from Business and Innovation Development (BID) unit of University of Turku, and a M.Sc. degree from Royal Institute of Technology (KTH), Sweden. He has a wide interest in embedded system design, adaptive systems, on-chip communication architecture, low-power and dependable computing. His current research is the integration of heterogeneous computing and communication systems, in particular concerning the collective adaptivity and timing predictability. Dr. Guang has served as PC members, session chairs and organizers of many international conferences, for instance HPCS2013, CASEMANS 2012, PECCS2013, etc. He is on the editorial board of IJERTCS. He has published over 40 papers and articles in international conferences and journals.

Juha Plosila is an Associate Professor in Embedded Computing at University of Turku (UTU), Department of Information Technology. He received a PhD degree in Electronics and Communication Technology from UTU in 1999. Plosila is the leader of the Embedded Computer and Electronic Systems (ECES) research unit and a co-leader of the Resilient IT Infrastructures (RITES) research program at Turku Centre for Computer Science (TUCS). He also leads the Embedded Systems master's program at the EIT ICT Labs Master School and is a management committee member of the EU COST Actions IC1103 (MEDIAN: Manufacturable and Dependable Multicore Architectures at Nanoscale) and IC1202 (TACLe: Timing Analysis on Code Level). Plosila is an Associate Editor of International Journal of Embedded and Real-Time Communication Systems *(IGI Global) and is regularly serving as a peer-reviewer, committee member, or guest editor for international conferences and journals. His current research deals with adaptive network-on-chip (NoC) based parallel embedded systems at different abstraction levels, with a special focus on emerging 3D stacked multiprocessor systems. This includes e.g. specification, development, and verification of self-aware, multi-agent monitoring and control architectures for massively parallel 2D/3D NoC systems, as well as applications of autonomous energy-efficient architectures to new computational challenges in the cyber-physical systems domain.*