International Journal of Cognitive Informatics and Natural Intelligence
Volume 14 • Issue 3 • July-September 2020

Optimizing for High Resolution ADC Model With Combined Architecture

Wei Ding, Key Laboratory of Earthquake Geodesy, Institute of Seismology, China Earthquake Administration, China
Heng Liu, School of information and Management, Guangxi Medical University, China
Tao Wu, Key Laboratory of Earthquake Geodesy, Institute of Seismology, China Earthquake Administration, China

ABSTRACT

High resolution analog-digital conversion (ADC) is a key instrument to convert analog signals to digital signals, which is deployed in data acquisition system to match high resolution analog signals from seismometers systems. To achieve high resolution, architecture of Σ-△ oversampling or pipeline ADC architecture have following disadvantages: high power consumption, low linearity of modulators, and complex structure. This work presents a novel model architecture, which design principle is validated by mathematical formulations which combined advantages of both pipeline and Σ-△oversampling ADC architecture. By discussing the adverse effects of the whole ADC architecture with an external noise theoretically, an amended theoretical model is proposed according to the assessment result of a noise simulation algorithm. The simulation results represent that the whole performance of combined architecture is determined by the noise level of integrator and subtractor. Using these two components with a noise index no more than 10-7 V/$\sqrt{}$Hz, the resolution of the prototype can achieve a reservation of 144.5 dB.

KEYWORDS

Analog-Digital Conversion (ADC), Architecture, Data Acquisition System, Matlab, Noise Analysis, Pipeline, Simulation, Σ-△Modulation

INTRODUCTION

Large bandwidth and wide power dynamic range are the two experimentally identified characteristics of free oscillations of the Earth (Woodhouse, 2013). The minimum probed displacement using seismeter is about accuracy of 0.1nm. The dynamic range of major earthquake is 220dB, whose range of bandwidth is from 10^{-5} Hz to 103Hz. Recording propagating seismic waves can be employed to analyze the Earth's interior (Curtis, 2009). One of requirements of geophysical instrument is detecting and recording shakes of 1nm-10mm in bandwidth of 0.01-10Hz. To collect abovementioned seismic signals with various distance and power, the dynamic range of seismic data acquisition system should exceed 120dB (Shapiro, 2015). High resolution data acquisition system with slow sample rate is hard to achieve due to its volume of code (Doerfler, 2013) To record earthquake with various distances and magnitudes, the dynamic range of seismic data acquisition system should be further improved. A seismic instrument is constituted by seismometers, which is used to collect analog signals, and

DOI: 10.4018/IJCINI.2020070106

data acquisition system, which is employed to convert analog signals to digital signals for analysis. The noise level of seismometers is about 1uV when output voltage is ±20V, e.g., the dynamic range of ultra-wideband JCZ-1 seismometer and its successor - very broadband seismometer CTS-1 has exceeded 140dB (Cai, 2007, Cai, 2004). The dynamic ranges of high-resolution seismometers are more than 150dB, e.g., KS-2000 and CMG-40T, (Zeng, 2014). However, common data acquisition system can only achieve signal and noise rate (SNR) of 135dB at 50SPS (sample per second), there is the gap between the dynamic range of data acquisition system and the requirements of seismometer, which will cause low SNR and missing key seismic information stored in seismic wave. The limit of the resolution of data acquisition system can cause inaccuracy results of local measurements for geological and earthquake information.

To improve dynamic range of seismic data acquisition system, high resolution analog - to - digital conversion (ADC) should be employed in it. The resolutions of ADC have developed from 8-bits to 24-bit. Theoretical value of ADC dynamic range of with single 24-bit chips can achieve 144dB. But the realized data acquisition system with single 24-bit ADC only has low dynamic range, i.e., no more than 100-120dB (Bulgakov, 2001, Nash, 2012). 32-bit ADC electronic components have been developed, such as ADS1263 of Texas Instruments (TI) and LTC2500. However, the noise level can't satisfy the requirements of seismic data acquisition system. Since the geological environments are commonly unpredictable, an optimal solution that uses high resolution seismic data acquisition systems to minimize noise and improve resolution (Vigh, 2014). According to Nyquist sampling theorem, Nyquist-rate data converters are achievable, e.g., successive approximation (SAR) ADC, time intersects ADC, and folding ADC (Huang, 2013, Namgoong, 2015). The convertible rate of abovementioned ADC is equal to Nyquist sample rate. However, the non-ideal conditions of circuit and component matching cause low resolution of Nyquist-rate ADC, which cannot exceed 120dB (Tual, 2016). To realize high resolution ADC for data acquisition system, Σ-△ oversampling and pipeline architecture ADC are needed. The detail principles of those two ADC architectures are elaborated in next section.

Using Σ-△ oversampling and pipeline architecture ADC to improve resolution separately can lead following problems: increased power consumption, reduced linearity of modulators, and increased complexity of circuit structure, and the resolution of whole system cannot be regulated easily. To solve abovementioned problems, some mathematical formulations combined pipeline and Σ-△ oversampling architecture principles are presented in high resolution data acquisition system. A simple and mathematical combined ADC model is amenable to analysis is presented. This paper analyzes theoretically the various sources of noise by this model. A further amended model based on analyzed results is verified by simulation of Matlab/simulink. The results represent that noises level of integrator and subtractor in first level determine the whole performance. To promote the implementation resolution, low outside noise device should be used for substractor and integrator. At 1V reference with the power supply of 3.3V, the ADC model achieves reservation resolution of 150 dB.

This paper is an enhance version of our previous work published in proceedings of the ICCICC 2019 conference. The remainder of this paper is organized as follows. In Section background, we describe the related works for research and application of high-resolution ADC. The design principle and research method for the model are presented in Section combined architecture for high resolution ADC. Section model implementation discusses implement of the model. Section results and discussion presents the simulation results and discussions of method for improve ADC resolution. The conclusions and future research directions are outlined in Section conclusion.

BACKGROUND

Works for Σ-△ Oversampling ADC Architecture

The design principle of Σ-△ oversampling ADC is elaborated below: △ is from the difference from the analog input signal and the output of DAC. Σ is the turn the result of △into integral. The result

compared with reference voltage will determine whether or not the output of 1-bit ADC is high. To improve resolution of ADC, the output stream is smoothed by digital filtering, which is the basis of oversample technique. The theoretical maximum multiples of Σ-△ modulator are 64-256 multiples to convert rate (Shu, 1995). Based on variables analysis in Equation 1, an effective method to enhance resolution of Σ-△ modulator, i.e., SNR_{dB}, is to increase order of the loop filter L. Additional integrators and feedback paths can be added to the basic of first order modulator (Johnston, 2001). The improvement goal of ADC performance is to modulate noise band in high frequency and reduced noise in special bandwidth via noise shaping and oversample techniques. Using digital decimation filter, the output frequency is reduced to signal bandwidth. Set modulator is L order and quantization bit is B, SNR of modulated quantization noise can be represented as Equation 1:

$$SNR_{dB} = 20\lg\left(2^{B}-1\right)+1.76+10\lg\left(\frac{2L+1}{\pi^{2L}}\right)+10\left(2L+1\right)\lg\left(OSR\right) \tag{1}$$

If we increase order L or quantization bit B, the performance of modulator can be improved when over sampling rate (OSR) is increased. For example, when L is equal to 4, the SNR is higher 21dB than that of L is 3. But SNR cannot be improved endless by enhance L. The reason is that the higher L is, the modulator will be more unstable and costs of circuit are higher.

Works for Pipeline ADC Architecture

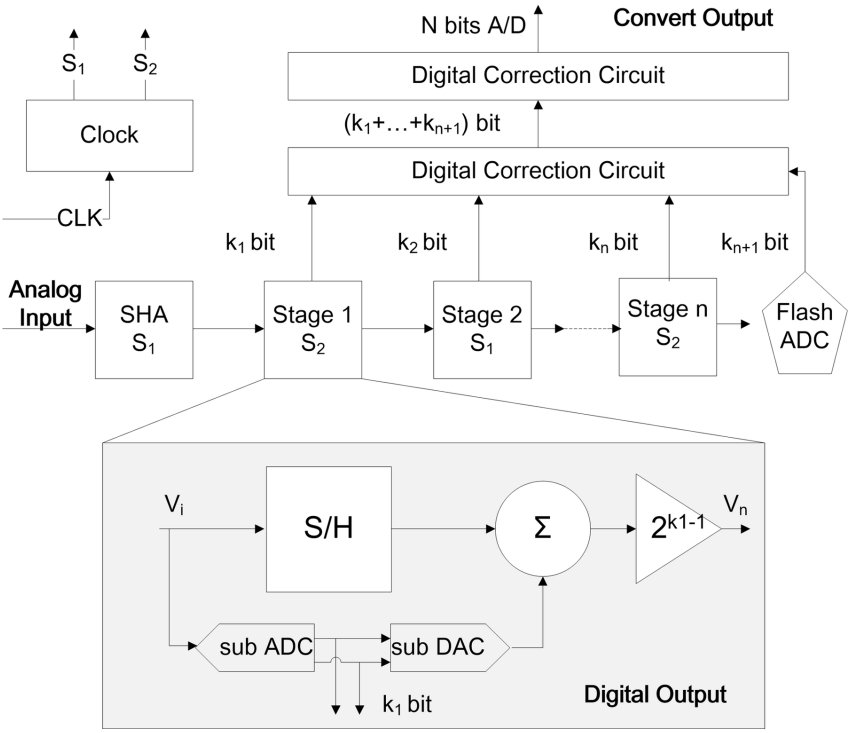
The principle of pipeline ADC is elaborated in Figure 1.

Pipeline ADC is composed of multistage with the same circuit structure. The key module is pipeline convert module which located in first order to compose of sample/hold (S/H) circuit, low resolution convertor, substract, and gain amplifier (Ginés, 2017). The principle of pipeline ADC architecture is elaborated as below: The whole data converting process is composed with 3 parts: analog input, digital output and convert output. As shown in Figure 1, bit convertor is carried out in primary order, then digital signal is subtracted from sample signal, and the result is the input for next level order. Signals convert in low bit are carried out in primary order and those in high bit are carried in high level order. The final digital signals are converted via iteration conversion method. Set the order i as example, clock circuit generates dual clocks CLK to control sample module and amplifier module separately. Sample and hold (S/H) circuit samples analog input signals in sampling phase, and transfers them to the next order as input voltage V_i in holding phase. Sub-ADC converts V_i to digital signals. k_1 bits from digital signals are stored in delay memory array and as digital input for sub-DAC. V_i is difference between input and analog quantity passed through K_1 bits, the result will be amplified 2^{k1-1} multiples. In order i, the word length of sub-ADC and sub-DAC are K_i, the amplified results of residues difference are 2^{ki-1}, the effective resolution can be accumulated K_{i-1}. N is the resolution of whole pipeline ADC architecture, which can be calculated by following Equation 2:

$$N=K_1+K_2+\ldots K_n-n+K_{n+1} \tag{2}$$

For example, in 12 bits pipeline ADC, V_i is quantified to 3 bits data by first level ADC. The result will be input to 3 bits DAC. The difference between V_i and output of 3 bits DAC will be amplified 4 times and transfer to second level ADC. The abovementioned iterative process will break until the final level using 4 bits ADC. In one sampling time, convert results are got in all levels in different times. Therefore, the shift register should be set or cleared to calibrate time of each level. The advantages of pipeline are obvious: (1) parallel process promote the transfer efficiency; (2) To enhance resolution of pipeline ADC, only need to provide more transfer levels; (3) Using input SHA, high frequency can be sampled.

Figure 1. The principle of pipeline ADC



The major shortcomings of pipeline architecture are: voltage reference and offset circuits are too complex to be comparable in ideal accuracy, pretreatment for pipeline delays of input signal must be done, and satisfied the requirements of strict latches. Any ill-considered circuit design will decline the resolution of whole ADC architecture significantly.

Utilizing individually Σ-△ oversampling ADC architecture or pipeline ADC architecture cannot realize the resolution of 24-bit ADC (144dB). For examples, Kong et al found the resolution of data acquisition system employed 24-bit electronic component is 19.6 bits (Kong, 2015). Nguyen et al used a Σ-△ ADC with a hybrid tuning circuit to adjust RC time constant, this ADC achieves 106dB SNR (Nguyen, 2005). Zeng et al used 24-bit electronic component in 2kHz signal bandwidth, the SNR is 129.35dB and related significant bits are 21.2-bit (Zeng, 2015). Schreier et al use fourth-order continuous-time technique to design a quadrature bandpass delta-sigma ADC with total dynamic range of 90dB (Schreier, 2006). In seismic field, mainstream seismic data acquisition systems are based on 24-bit ADC electronic components of Σ-△ oversampling architecture, e.g., EDAS-24GN of Gangzheng co., ltd, TDE-324 of Taide co., ltd, and 130 series of Reftek co. ltd, which dynamic ranges are 135dB. To exceed the limit of 144dB, an innovated ADC model with new architecture is needed.

Researchers also propose various methods to promote SNR of ADC. For example, Kimura et al use a delta-sigma modulator to reduce the effects of clock jitter and adjust loop delay with a vector filter (Kimura, 2013). The improvement of SNR is 84.5dB, which is 22.5dB higher compared to SNR of a conventional ADC. Wang et al employ differential input programmable gain front end changes from 1 to 128, so that the weak voltage signals can be directly transferred from analog sensors (Wang, 2018). The presented ADC can achieve 20 bits of resolution with sampling clock of 19.5kHz. Wang et al. present a current mode capacitively-coupled chopper instrumentation amplifier embedded delta-sigma ADC (Wang, 2017). The input referred noise can achieve 128dB via chopper-stabilized

current-mode. As our knowledge, the abovementioned methods cannot directly promote the SNR of ADC exceed the limitation of 144dB.

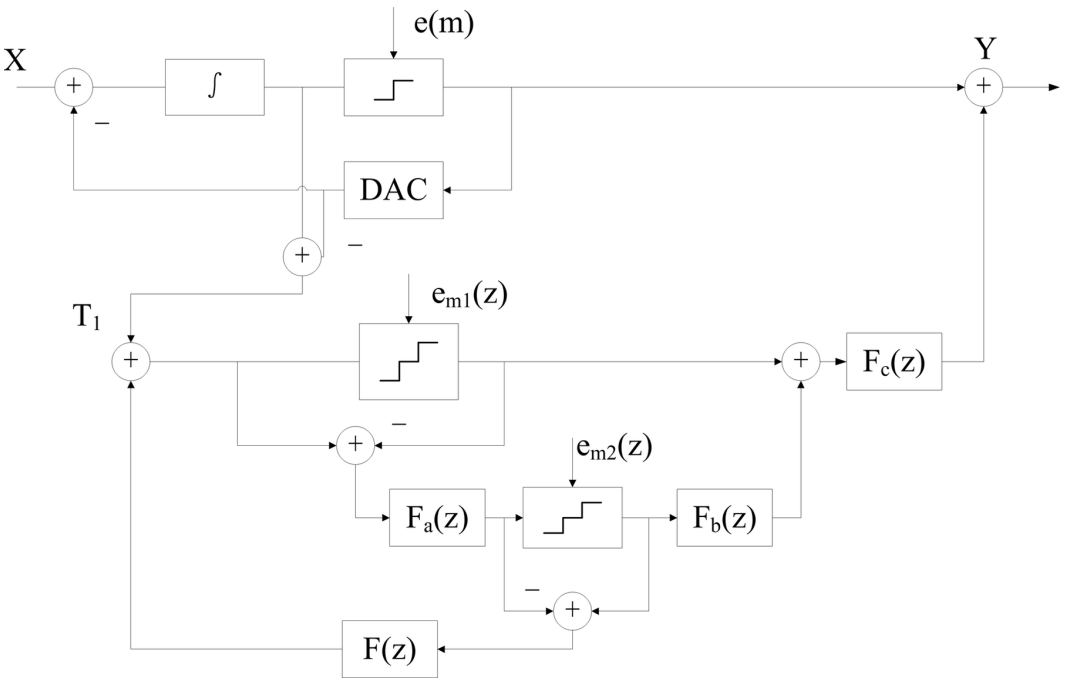
Computer simulation has been used to verify the characteristics of ADC in different application. For example, In Kimura's work, the clock with jitter, white noise, and time delay are generated and verified in MATLAB/simulink (Kimura, 2013). Schreier et al use computer simulation to determine the stability of 1 bit Σ-△ modulators up to order 8 (Schreier, 1993). Maximum SNR are plotted and oversampling rate is presented. Posselt et al. used mixed-signal orthogonal frequency division multiplex system simulation to evaluate a frequency agile direct RF ADC. The method allows flexible testing of different ADCs and analyzes the noise of ADC (Posselt, 2015). The necessary steps of the signal process and combination influence of noise shapes are testified on multi-domain. In our work, we also use Matlab/simulink simulation to agile develop the model of ADC and verify the performance of combined model.

COMBINED ARCHITECTURE FOR HIGH RESOLUTION ADC

Design Principle

To improve the resolution of ADC, an architecture for ADC model combined pipeline and oversampling is presented (KinYua, 1999). It is composed of two orders. In first order, simplified Σ-△ ADC architecture is used for receiving analog input signals. To reduce noise, the integrated result of single bit signal is calculated and compared with reference voltage, then output single bit DAC. In second order, pipeline ADC architecture is used to accumulate the incremental signals to improve resolution. The maximum amplitude of noise will be eliminated in first order and the rest noise will be reduced via these methods. The detailed design principle and the proposed noise shaping technique are elaborated in Figure 2 as below:

Figure 2. The model structure combined pipeline and Σ-△ oversampling ADC architecture



The signals transferring possess in first order is elaborated as below: input signal X and noise e_m should be considered separately. Single bit DAC is an optimal line which gain is 1. The whole circuit is a single-feedback closed-loop system. One single bit DAC is used for a comparator to transfer analog signal to various low or high electrical level. The role of integrator is described as following: accumulate the difference between signals and output of DAC. The transfer functions of the first integrator will be $H(z)=z^{-1}/(1-z^{-1})$. The signal can be presented by $Y_{s(z)} = \frac{H_{(z)}}{1+H_{(z)}} X_{(z)}$. The noise can be regarded as a white noise source generated from two bit selectors structured by voltage-controlled switch. The noise will be transferred via two paths, transferring function of one path is 1, another is negative feedback with integrator H(z). Transfer function of noise can be calculated by $Y_{n(z)} = \frac{1}{1+H_{(z)}} e_{(z)}$, and the total transfer function of first order can be substituted and simplified as follow:

$$Y_{(z)} = \frac{H_{(z)}}{1+H_{(z)}} X_{(z)} + \frac{1}{1+H_{(z)}} e_1(z) \tag{3}$$

As shown in Figure 2, modulator with e_m noise in first order is the basic of whole circuit. The signal added procession in second order can be presented in Equation 4:

$$y(z) = x(z)z^{-1} + e_1(z)\left(1-z^{-1}\right) + \left(e_m - e_1\right)F(z) \tag{4}$$

Note that, the quantization noise can be eliminated via selective parameters of filters $F_{(z)}$, i.e., Let $F_{(z)}=(1-z^{-1})$.

The simplified y(z) which eliminated quantization noise e_1 is shown in Equation 5:

$$y(z) = x(z)z^{-1} + e_m\left(1-z^{-1}\right) \tag{5}$$

When the potential maximum noise e_1 is eliminated, quantization noise e_m generated by ADC of second order still can be reshaped. In the subsquent process, we describe how pipeline topology in Figure 2 to reduce noise, i.e., residual signals generated in first order are filtered and shaped in next order. For example, the input signal is 1.13V, quantization DAC is 16 bits, i.e., $2^{16} = 32768$, and reference voltage is 2.5V. The actual voltage should be 1.13*32768/2.5 = 14118.136. However, DAC only can convert voltage to integer, e.g., 14118 or 14119, which will cause error with 1 count. The difference between actual value and converted value of DAC is the reason for decreasing resolution of our ADC model, which will be discussed in next section.

Model Structure for Combined Pipeline and Oversampling ADC Architecture

A further analysis of model structure based former design principle is described in this section. As we have discussed in abovementioned paragraph, output y(z) can be calculated as below:

$$y(z) = x(z)z^{-1} + e(z)\left(1-z^{-1}\right) + \left\{e_{m1}(z)\left(1-F_aF_b\right) + e_{m2}(z)\left(F_b - F\right) - e(z)\right\}F_c(z) \tag{6}$$

F, F_a, F_b and Fc are selective filters for our model in Equation 6. To eliminate quantization noise e_1 and e_m, the filters' parameters are well-designed for counteracting $F_a(z)$ and $F_b(z)$.

Equation 6 can be further simplified to Equation 7 by using chosen parameters:

$$y\left(z\right) = x\left(z\right)z^{-1} + e_{m2}\left(z\right)\left(1 - z^{-1}\right)^2 / k \tag{7}$$

In Equation 7, we can identify following characteristics of the model: the two major quantization noises $e_1(z)$ and $e_{m1}(z)$ are eliminated by well-designed structure; Using third order modulation, another quantization noise $e_{m2}(z)$ is handled as small as possible to maximize. By this means, the whole ADC model SNR is improved fundamentally.

MODEL IMPLEMENTATION

Modified Model Structure With Outside Noise Sources

In practical use, inherent noise of each part in ADC architecture should be considered. Design principle of ideal model combined pipeline and oversampling ADC architecture in previous section. Various outside noises should be considered in practice on the basis of ideal combined architecture. Table 1 describes difference types of outside noises from electronic components

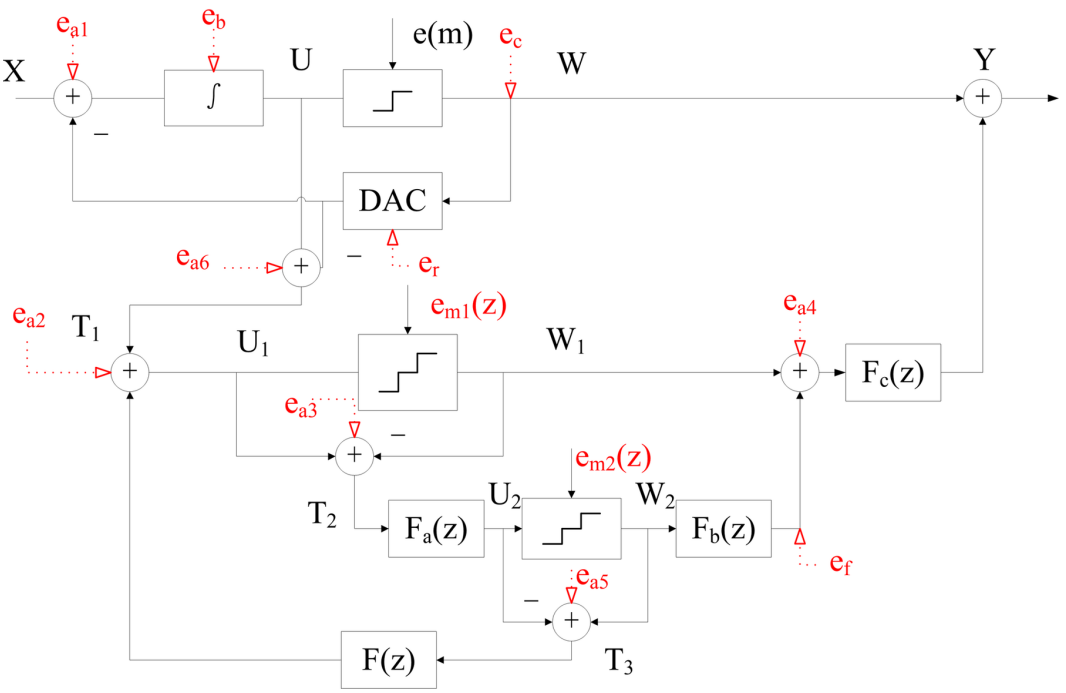
Table 1. Outside noises for model combined pipeline and oversampling ADC architecture

Noise Name	Description	Typical Electronic Device	Noise Level
e_{a1}- e_{a6}	Noise from subtractor, which is generated by amplifiers and their peripheral circuit	OP140	9nV/$\sqrt{}$Hz
e_b	Noise from integrator, which is generated via amplifier and its peripheral circuit	AD620	9nV/$\sqrt{}$Hz
e_c	Noise from zero-crossing comparator, which is generated by several amplifiers and their peripheral circuit	AD620	9nV/$\sqrt{}$Hz
e_r	Noise from reference voltage, which is generated from power supply ripple	LTC6655	9nV/$\sqrt{}$Hz
e_{m1}-e_{m2}	Noise from ADC electronic components in second order	ADS8681	100dB
e_f	Noise from Logic array, which is generated from FPGA electronic component	Altera Cyclone IV	123 dB/Hz

except for the discussed noises in ideal model. Noise names and their description are directly shown in the first two columns. Typical electronic components and their noise level declared in datasheet are elaborated in last two columns of Table 1. The input voltage noise density and current noise density are the key reference noises for each electronic device, which are described in datasheets of investigated devices.

To consider abovementioned noises, Figure 3 shows the practical model combined pipeline and oversampling ADC architecture. The external noises and their affected components are represented by red dotted arrows. In the next section, a simulation algorithm to evaluate the effect of external noise is presented based on graphical representation of Figure 3.

Figure 3. Modified model structure with outside noise sources



Simulation Algorithm

A simulation model with external noise based on Matlab is performed to integrate various outside noises and signals as a whole. The model is composed of three modules: one order DAC to eliminate noise $e_1(z)$ based on Σ-△ ADC architecture, two order DACs collect the converted analog values and store and describe them in a digital file. The last state is stored synchronously in storage based on pipeline ADC architecture. Digital values of voltages collected in each order are merged to final output. Table 2 shows simulation algorithm and their corresponding annotation using Matlab. Psedo codes and their belonged architecture model are directly shown in the first two columns. Detailed annotations for each line of code are elaborated in last two columns of Table 2.

RESULTS AND DISCUSSION

Simulation Result

Actual codes are implemented by Matlab/simulink based on the design principle in previous section. Figure 4 presents the results of simulation based on pseudo-code. As shown in Figure 4, (a) and (d), input signals and its amplification, i.e., a sine wave which frequency is 50 Hz and related sample rate is 8KHz. (b) and (e) present the output signals and its amplification through the ADC model combined pipeline and sigma-delta oversampling architecture separately. We can find the distortion of output sine signal caused by various noises in Figure 4 (e). Note that, sine signal is amplified partially and shown in Figure 4 (d) and (e) so that the effect caused by various noises can be displayed. Figure 4 (c) presents single-sided amplitude spectrum of signals and noises and (f) shows the magnified version. Amplitude spectrum is defined in terms of the magnitude of the Fourier transform, which can be used to quantities the units of volts per Hz (Aki, 2012). The amplitude of 50Hz Signal is clearly shown in Figure 4 (c). Meanwhile the amplitude of noise cannot be shown in Figure 4 (c) directly

Table 2. Simulation pseudo code and their annotation using Matlab for model combined pipeline and oversampling ADC architecture

Architecture Model	Psedo Code	Annotation
Σ-△ oversampling ADC architecture	$U_{ref}=U_{ref}+e_r$;	the noise of reference voltage should be considered first
	$U=(X-W_0)+e_b$;	z^{-1} means last state of z, hence we consider e_b
	If U>0, $W=U_{ref}+e_r+e_c$;	W is the output of first order and its related noise
	Else $W=-U_{ref}+e_r+e_c$;	e_c is the noise from zero-crossing comparator, which will effect U_{ref}
	A1=W*FSC;	A1 is the result of converting the highest bit of W to digital
	E=W-U;	
	$T_1=U-W+e_{a6}$	
Pipeline ADC architecture	$U_1=T_3F(z)+T1+e_{a2}$;	
	$U_2=T_2Fa(z)$	
	$W_{1temp}=[U_1+e_{m1}(z)]*FSC/U_{ref}$;	Using proportion to convert W_1 to digital
	$W_1=\{W_{1temp}\}_R*U_{ref}/FSC$;	Subscript R means rounding voltage result, which will be stored and used in next order
	$A_2=\{W_{1temp}\}_R$;	Subscript temp means temp single for further processing
	$T_2=U_1-W_1+e_{a3}$;	
	$W_{2temp}=[U_2+e_{m2}(z)]*FSC/U_{ref}$;	
	$W_2=\{W_{2temp}\}_R*U_{ref}/FSC$;	
	$A_3=\{W_{2temp}\}_R*F_b(z)$;	Rounding voltage used in next order, i.e., it's the source of error for converting analog to digital
	$T_3=W_2-U_2+e_{a5}$;	
	$Y=(A_1(k)+(A_2(k)+A_3(k)-F_z))/FSC$;	
	$F_z=A_2(k)+A_3(k)$;	Cycle storage for state of F_z, which is a standby for next loop
	Fouler (F_z);	Fourier transform of F_z to calculate the dynamic range and related SNR
	Back to start	Loop and begin another collection process

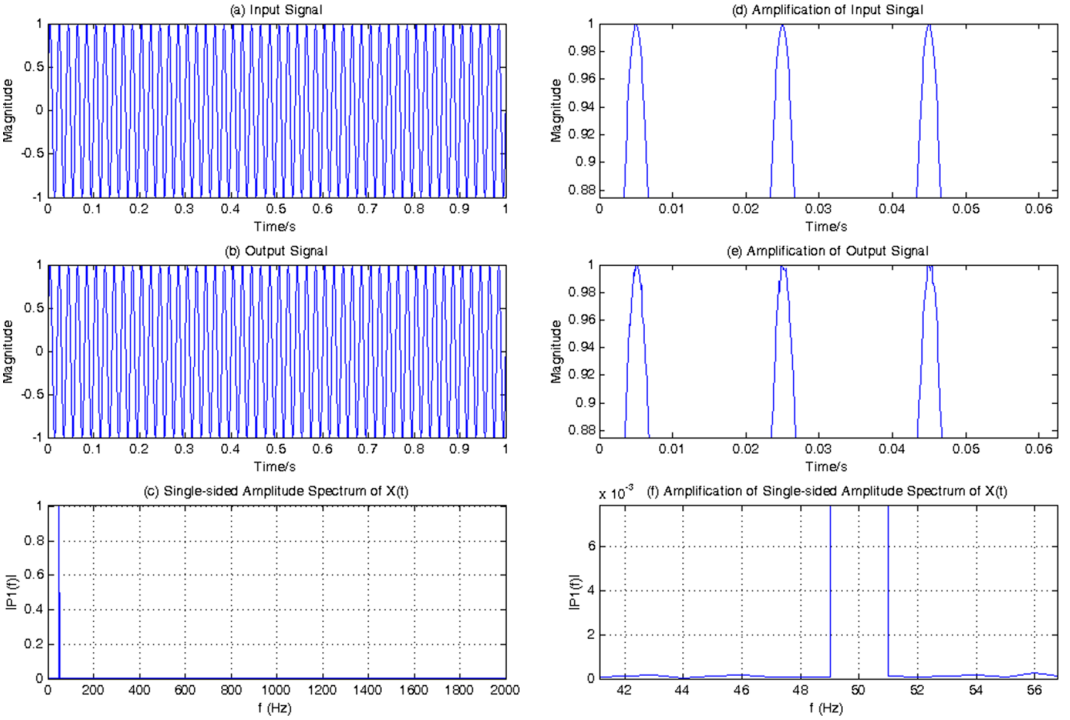
for its magnitude is too small to display with signal. We present the magnified white noise in Figure 4 (f). SNR can be calculated with Equation 8:

$$20\log_{10}(S/N) \quad (8)$$

For example, amplitude of noise in Figure 4 (d) is $0.8*10^{-4}$V. The correspondent signal S=1 and $N=0.8*10^{-4}$ can be substituted to Equation 8 and calculate that SNR is 81.94dB. SNR in various parameters is calculated iteratively during the calculation process.

As discussed in section background, model combined pipeline and Σ-△ oversampling ADC architecture have been advocated in section design principle and its pseudo-codes are shown in section model structure. Various types of noise are analyzed in this section based on the ADC model and its pseudo codes. By adding various outside noises, signals transfer process can be simulated. By study the degree of importance for each outside noise, we try to identify the influence factors for outside

Figure 4. Results of Matlab simulation



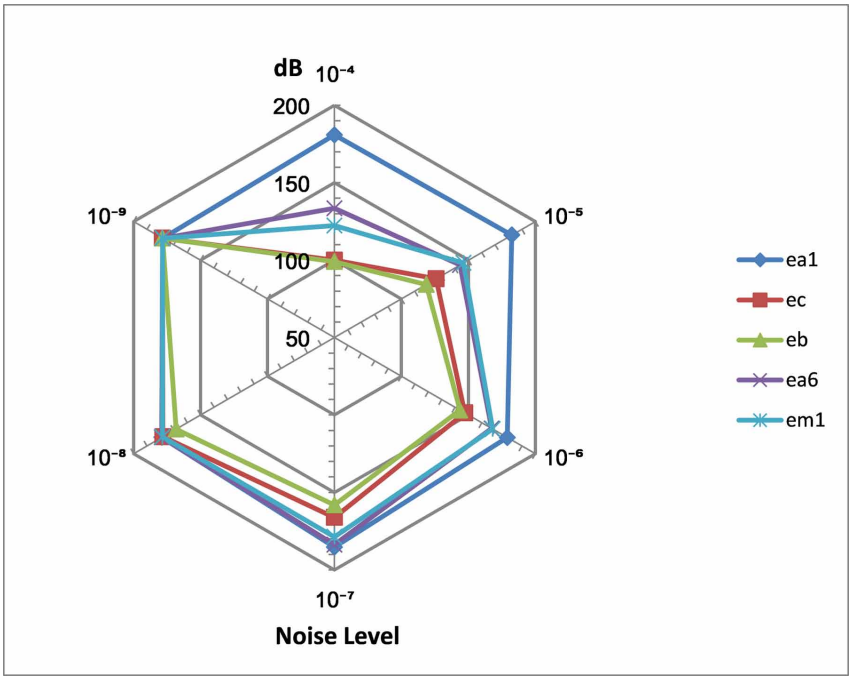
noise. Noise spectral densities (NSD) of outside noise are used to specify characteristic of outside noise. The unit of noise spectral density is V/$\sqrt{}$Hz, i.e., 1V noise voltage per $\sqrt{}$Hz. For example, if the NSD is 30nV at 100Hz bandwidth, the value is 0.3uV in 10kHz. By using the data of column noise level in Table 1, announced noises in datasheet for each component are substituted in our simulation program to calculate the SNR. The analysis results are elaborated in Table 3 and Figure 5.

Table 3. Simulation results between outside noises level of various noise and ideal SNR for combined architecture

Noise Name	External Noise for Various Outside Noise Level (dB, V/$\sqrt{}$Hz)					
	10^{-4}	10^{-5}	10^{-6}	10^{-7}	10^{-8}	10^{-9}
e_{a1}	180.92	182.5	179.09	185.35	178.94	178.42
e_c	100	125.93	147.33	166.19	178.13	178.42
e_b	99.07	118.62	143.65	158.06	168.24	178.42
e_{a6}	133.48	143.81	167.41	183.74	178.94	178.42
e_{m1}	122.36	146.41	168.18	178.71	178.42	178.42

Table 3 shows the final SNR (units: dB) of combined architecture when difference types of outside noises are changed. Noise names are directly shown in the first columns. Typical electronic components and their noise level using in Matlab simulation are elaborated in the first and second lines of Table 3. For example, a selected component with 10-6 noise level for e_b will make the whole system's SNR to 143.65dB. Figure 5 uses a radar map to show the relationships between difference

Figure 5. Relationships between various level of outside noise and SNR



noise level of outside noise and SNR. Table 3 shows numerical value for each dot elaborate in Figure 5. Various noise sources are represented by different lines with special mark in Figure 5, e.g., noise e_c is represented by line with squares dot. Regular hexagon border with grey lines represent different SNR of ADC architecture, e.g., from outside to inside, the second regular hexagon means 150dB. If result dot is outside the hexagon border, it means the result is beyond 150dB, and vice versa, it's below 150dB. To identify the effect of separate noise source, only one noise level for each noise source is changed when the simulation program is performed.

Principle Prototype

Using the abovementioned ADC architecture, a principle prototype of data acquisition system based on combined pipeline and oversampling ADC architecture is represented in Figure 6. The data acquisition system consists of three layers PCB structure from bottom to top: power supply layer, ADC architecture layer, and signal processing layer. In this prototype, the ADC architecture layer and partial signal processing layer are based on the theory advocated in this work. After short the input ends of data acquisition system, we can calculate the SNR for the whole system is about 144.5dB, which is increased SNR by 9dB to former system.

Discussion

This experiment focuses on how to realize high resolution ADC model, i.e., more than 144dB (about 24 bit ADC). Figure 5 presents the following findings:

- **Key noise sources:** Figure 5 presents the trends of decline for SNR when the noise level is change for different noise source. For example, SNR is maintain about 180 dB when the ea1 changes from 10-9 to 10-4 V/$\sqrt{}$Hz, i.e., the blue square dot are all near 180dB. As we have discussed in Section, the reason of this result is that eea1 is the part of $e_{(m)}$, which have been eliminated via

Figure 6. Principle prototype of data acquisition system based on combined pipeline and oversampling ADC architecture

selective parameters of filters $F_{(z)}$. As shown in Figure 5, the two types of important noise sources are e_b and e_c, whose SNR reduces rapidly when the noise level exceeds 10^{-7} V/$\sqrt{}$Hz. This means that those two noise sources, i.e., e_c and e_b are the key noise sources affected SNR of our model. The reason of this result is that both noise sources are in first order and cannot be eliminated subsequent iterations procession easily, which will be amplified or generate self-excitation in second order based on the model principle elaborated in section design principle;

- **The requirements of noise level:** The model is designed for realizing ADC with high resolution, i.e., the value of SNR should exceed 144dB for single 24-bit ADC chip. It means all outside noise for every source must be less than 10^{-7} V/$\sqrt{}$Hz. As shown in Figure 5, if high level outside noise is employed, i.e., exceeds 10^{-7} V/$\sqrt{}$Hz, SNR of whole system, which means the dots is beyond 150dB. The reference noise of selective electronic components in circuit, e.g., multi-bits ADC, amplifiers, and FPGA (Bai, 2017), must satisfy the requirements of noises. For example, low noise chips, such as OP140, is selected in first order for the model for its lower outside noise compared to other amplifier electronic components. Meanwhile, we can find that outside noises in same order are similar to others. For example, e_{a6} and e_{m1} change synchronously in Figure 5. The reason of this result is that both noise sources are based on pipeline ADC architecture in second order. Both two noise sources can be reduced by third order modulation to maximize as less as possible. As present in design principle section, outside noises cannot be entirely eliminated because there are no electronic components without self-noises in practices;
- **Various noises sources for combined model:** Different noise sources carry various weights in application of the combined ADC model, such as comparator, switched-capacitor, and multi-bit ADC (Sepke, 2009). The noise of comparator from virtual ground dominates the overall noise performance of the ADC model. Size of capacitor for reference current, whose contribution is small in simulation, and amplifiers of first order are critical for implement of this model. They can be managed through appropriate design and components selection.

CONCLUSION

To match the requirements of highly sensitive sensors in seismometers systems, data acquisition system should deploy high resolution ADC as key component, which can be used to improve resolution and accuracy of seismic dataset. As we have discussed in the previous session, existing ADC models

architecture based on Σ-△ oversampling or pipeline ADC will increase power consumption, reduce linearity of modulators and depend on complex circuit. To solve those problems for high resolution ADC, a simple and constructure combined pipeline and oversampling ADC model is presented. This paper analyzes theoretically the various noise sources by simulation model. A further amended model based on noise analyzed results is verified by proposed simulation algorithm. The results represent that noises level of integrator and subtractor in first order determine the whole performance, which can achieve reservation resolution of 150dB. A principle prototype is designed based on theory of this work. Its SNR reaches 144.5dB.

This work has illuminated several promising research directions that are underexplored in current research in practice:

1. Selecting proper high-performance devices to implement the circuit. The results show that at the proper condition, the advocated combined ADC model can achieve resolution of 150dB. But not all devices have their claimed noise levels, which cause the SNR of principle prototype is 144.5dB. Optimal devices for circuit should be selected after comparing to device with same type. The combined model which simplifies the designing of data acquisition systems with higher performance should be developed in the future work;
2. How to better apply simplified structure. As we discussed in model structure section, several components are used in ADC combined pipeline and oversampling ADC model. In practice, some components can be united to simplify structure even more, e.g., an integrator and a subtractor can be convert a united component, which can save an amplifier. We need more research on qualitative or quantitative on the costs and benefits of using this component.

ACKNOWLEDGMENT

This work is partially sponsored by the Scientific Research Fund of Institute of Seismology and Institute of Crustal Dynamics, China Earthquake Administration (Grant No. IS201726156), the National Natural Science Foundation of China No. 61866014, and Science Foundation of Jiangxi University of Science and Technology under Grant No. jxxjbs18059. Thank the ICCICC 2019 reviewers for their valuable comments to this work.

REFERENCES

Aki, K. (2012). Scaling law of seismic spectrum. *Journal of Geophysical Research*, *72*(4), 1217–1231. doi:10.1029/JZ072i004p01217

Bai, Y., Gaisbauer, D., Huber, S., Konorov, I., Levit, D., Steffen, D., & Paul, S. (2017). Intelligent FPGA Data Acquisition Framework. *IEEE Transactions on Nuclear Science*, *64*(6), 1219–1224. doi:10.1109/TNS.2017.2708510

Bulgakov, A. Y., V'yukhin, V. N., & Popov, Y. A. (2001). A 24-Bit data acquisition system. *Instruments and Experimental Techniques*, *44*(2), 180–182. doi:10.1023/A:1017554717595

Cai, Y., Lv, Y., Cheng, J., Yu, J., & Lv, P. (2007). Application of JCZ-1T Ultra Broadband Seismometer as an instrument for integrated observation. *Seismological and geomagnetic observation and research, 9*(5), 29-34.

Cai, Y., Lv, Y., Zhou, Y., & Chen, J. (2004). CTS-1 very broadband seismometer. *Journal of geodesy and geodynamics, 24*(6), 109-104.

Curtis, A., Nicolson, H., Halliday, D., Trampert, J., & Baptie, B. (2009). Virtual seismometers in the subsurface of the Earth from seismic interferometry. *Nature Geoscience*, *2*(10), 700–704. doi:10.1038/ngeo615

Doerfler, D. W. (2013). Dynamic testing of a slow sample rate, high-resolution data acquisition system. *IEEE Transactions on Instrumentation and Measurement*, *35*(4), 477–482. doi:10.1109/TIM.1986.6499120

Ginés, A. J., Peralías, E. J., & Rueda, A. (2017). Black-box calibration for ADCs with hard nonlinear errors using a novel INL-based additive code: A pipeline ADC case study. *IEEE Transactions on Circuits and Systems. I, Regular Papers*, *64*(7), 1718–1729. doi:10.1109/TCSI.2017.2662085

Huang, G. Y., Chang, S. J., Liu, C. C., & Lin, Y. Z. (2013). 10-bit 30-MS/s SAR ADC Using a Switchback Switching Method. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 21(3), 584–588. 10.1109/TVLSI.2012.2190117

Johnston, J. E. (2001). A 24-bit delta–sigma ADC with an ultra-low noise chopper-stabilized programmable gain instrumentation amplifier. *Computer Standards & Interfaces*, *23*(2), 123–128. doi:10.1016/S0920-5489(01)00066-6

Kimura, Y., Yasuda, A., & Yoshino, M. (2013). Continuous-time delta-sigma modulator using vector filter in feedback path to reduce effect of clock jitter and excess loop delay. *Analog Integrated Circuits and Signal Processing*, *75*(2), 279–286. doi:10.1007/s10470-013-0038-6

KinYua. M.K. (1999). Obersampled multi-bit Sigma-delta A/D Convberters. Master. Texas, USA: Texas Tech University.

Kong, F., Ding, G.-Q., & Chen, X. (2015). Design of multi-channel data acquisition based on ADS125x and related accuracy improving method. *International Electronic Elements*, *22*(8), 97–99.

Namgoong, M. A. W. (2015). Comparator Power Minimization Analysis for SAR ADC Using Multiple Comparators. IEEE Transactions on Very Large Scale Integration (VLSI). *Systems*, *62*(10), 2369–2379.

Nash E. (2012). Using the AD771x family of 24-bit sigma-delta A/D converters.

Nguyen, K., Adams, B., Sweetland, K., Chen, H., & McLaughlin, K. (2005). A 106dB SNR hybrid oversampling ADC for digital audio. In *Proceeding of IEEE International Digest of Technical Papers. Solid-State Circuits Conference (ISSCC)* (pp. 1-8). IEEE.

Posselt, A., Berges, D., Klemp, O., & Geck, B. (2015). Evaluation of a frequency agile direct RF ADC based on mixed-signal OFDM simulation. In *Proceeding of 26th IEEE Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)* (pp. 694-697). IEEE. 10.1109/PIMRC.2015.7343387

Schreier, R. (1993). An empirical study of high-order single-bit delta-sigma modulators. *IEEE Transactions on Circuits and Systems*, *40*(8), 461–466. doi:10.1109/82.242348

Schreier, R., Abaskharoun, N., Shibata, H., Paterson, D., Rose, S., Mehr, I., & Luu, Q. (2006). A 375-mW quadrature bandpass delta sigma ADC with 8.5-MHz BW and 90-dB DR at 44 MHz. *IEEE Journal of Solid-State Circuits*, *41*(12), 2632–2640. doi:10.1109/JSSC.2006.884340

Sepke, T., Holloway, P., Sodini, C. G., & Lee, H. S. (2009). Noise analysis for comparator-based circuits. *IEEE Transactions on Circuits and Systems*, *56*(3), 541–553. doi:10.1109/TCSI.2008.2002547

Shapiro, B., Kissel, J., Mavalvala, N., Strain, K., & Youcef-Toumi, K. (2015). Limitations of Underactuated Modal Damping for Multistage Vibration Isolation Systems. *IEEE/ASME Transactions on Mechatronics*, *20*(1), 393–404. doi:10.1109/TMECH.2014.2333715

Shu, T. H., Song, B. S., & Bacrania, K. (1995). A 13-b 10-Msample/s ADC digitally calibrated with oversampling delta-sigma converter. *IEEE Journal of Solid-State Circuits*, *30*(4), 443–452.

Tual, S. L., & Doris, K. (2016). Session 27 overview: Hybrid and nyquist data converters. In *Proceeding of 10th IEEE International Solid-state Circuits Conference (ISSCC)(*p.^pp. 454-455). San Francisco, CA, USA:IEEE. 10.1109/ISSCC.2016.7418103

Vigh, D., Jiao, K., Watts, D., & Sun, D. (2014). Elastic full-waveform inversion application using multicomponent measurements of seismic data collection. *Geophysics*, *79*(2), 63–77. doi:10.1190/geo2013-0055.1

Wang, H., & Mercier, P. P. (2017). A current-mode capacitively-coupled chopper instrumentation amplifier for biopotential recording with resistive or capacitive electrodes. *IEEE Transactions on Circuits and Wystems. II, Express Briefs*, *65*(6), 699–703.

Wang, Y., Liu, Y., Zhou, X., Wang, A., & Cao, B. (2018). An on-chip signal conditioning delta-sigma ADC for micro-mechanical gyroscope applications. In *Proceeding of 12th IEEE International Conference on ASIC (ASICON)* (pp. 48-51). IEEE.

Woodhouse, J. H., Giardini, D., & Li, X. (2013). Evidence for inner core anisotropy from free oscillations. *Geophysical Research Letters*, *13*(13), 1549–1552. doi:10.1029/GL013i013p01549

Zeng, J. Q. (2015). *Design and implementation of 24-bit Delta-Sigma A/D converter*. Beijing Jiaotong University.

Zeng, R., Lin, J., & Zhao, Y. (2014). Development situation of geophones and its application in seismic array observation. *Diqiu Wulixue Jinzhan*, *28*(5), 2106–2112.

Wei Ding is a senior engineer of Key Laboratory of Earthquake Geodesy, Institute of Seismology, China Earthquake Administration. His major research directions are seismic instrument and software engineering.

Heng Liu is an associate professor of School of information and Management, Guangxi Medical University. She is the corresponding author of this paper. Her major research directions are artificial intelligence and software engineering.

Tao Wu is an engineer of Key Laboratory of Earthquake Geodesy, Institute of Seismology, China Earthquake Administration. His major research directions are seismic instrument and electronic engineering.