An Extensive Power and Performance Analysis for High Dimensional Mesh and Torus Interconnection Networks

Faiz Al Faisal, Department of Computer Science and Engineering, Green University of Bangladesh, Bangladesh*
M. M. Hafizur Rahman, Department of Computer Networks and Communications, King Faisal University, Saudi Arabia
Yasushi Inoguchi, Research Center for Advanced Computing Infrastructure, Japan Advanced Institute of Science and Technology, Japan

ABSTRACT

The next generation parallel computers are the keys to achieve exascale performance, whereas sequential computers have already been saturated. In order to achieve this mighty target of exascale computing, one of the main challenges is the reduction of power consumption along with achieving suitable performance. Energy efficiency is a key feature to ensure the trade-off between the performances over the required power usages. Hence, to focus on those issues, the target of this article is to analyze the performance versus power usage trade-off for the conventional networks like- Mesh and Torus. High degree networks show much better performance than the low degree of networks. However, high degree networks require higher power usage for their high degree of interconnected links. This article showed that with zero load latency, the 3D Torus could show about 57.07% better performance than a 2D Torus. On the other hand, a 2D Mesh network requires about 24.22% less router power usage than the 3D Mesh, & 5D Torus requires about 66.8% higher router power usage than a 3D Torus network.

KEYWORDS

Estimation of Power Consumption, Latency, Mesh and Torus Network, Routing Algorithm, Static Network Performance, Throughput, Traffic Patterns

INTRODUCTION

The plausible solution to meet the high computational demand is the modern supercomputers, which is also the center focus for many research areas (Yin, J. et al., 2019). One of the finest and foremost examples of supercomputers have recently been used to train, scale and accelerate the Morpheus Machine Learning Model, which is a convolutional neural network that helps to explain the color images of the distant universe provided by the James Webb Space Telescope (JWST) (Morpheus ML Model, n.d.). A NVIDIA graphics processing unit-enabled supercomputer, Lux, at the University of California, Santa Cruz, was used to train the Morpheus model having 80 CPU-only compute nodes and 28 GPU-only nodes. On the other hand, modern supercomputer Fugaku is being used to search...
for coronavirus treatment (used Tofu interconnect, Ajima, Y. (2018) and Y. Ajima et al. (2012)). Fugaku used A64FX microprocessor, which can achieve about 415 PFLOPS requiring about 28,335kW power usage (Kodama et al., 2020; Kudo et al., 2020). However, along with high performance, key to achieve the exascale performance is to ensure the high performance over power usage. Table 1 shows the recent green listed supercomputers (Vikram, 2015), where the recent MPC systems like-Gyoukou ensures the maximum petaFlops/megawatt efficiency of 14.14 (about 42.88% better than the Piz Diant). Therefore, performance per watt of the MPC systems is prime concern for the next generation supercomputers with other constraints like- low network performance, low scalability, low throughput, and latency (Sanchez et al., 2010).

The performance as well as power usage of a supercomputer highly depends on its inter-connectivity between the core-to-core, chip-to-chip, node-to-node and rack-to-rack. This inter-connectivity between various levels of networks is called as the “Interconnection Network” (Minkenberg, 2013). In case of power usages, the on-chip interconnection networks consume about 50% of the total power and off-chip bandwidth is limited to the total number of outgoing physical links (John, 2007). In modern supercomputer, on-chip networks are usually considered with electrical interconnects for their low power usage and off-chip networks are considered with optical interconnects, which are connected through the GBIC Modules for the high-speed connectivity (Pavlidis & Friedman, 2007). This research considered the conventional interconnection networks and extensively analyzed the power usage, network performance, and also investigated the effects of virtual channels in case of performance and power usages.

The later part of this paper describes the network structure of Mesh and Torus network, reviews the routing algorithm, illustrates the static network performance, compares the dynamic communication performance (DCP) for various networks, estimates the on-chip power consumption, and finally performance & power requirement analysis with increased virtual channels.

**BACKGROUND**

Green computing ensures the eco-friendly use of computers and their resources. It can be explained as the designing, using, and disposing of computing equipment in a way to minimize their environmental impact (Green500 List, n.d.; Vikram, 2015). Low energy consumption not only helps to minimize the running cost but also reduces the environmental impact of powering the computer (Al Faisal et al., 2021; Pavlidis & Friedman, 2007). In 2016, the many-core accelerators PEZY-SCnp at RIKEN achieved 6673.8MFLOPS/w power efficiency (Fu, 2016). On the other hand, according to the current analysis on Green500 list in November 2020, Preferred Network’s (PFN) Supercomputer MN-3 can achieve about 26.039 GFlops/watts power efficiency and requires about 65.39kW of electrical power having linkpack performance of 1,652 TFlop/s ranked as second, whereas NVIDIA DGX SuperPOD with 26.195 GFlops/watts is ranked as first having 19,840 cores (Green500 List, n.d.).

The Torus network shows better dynamic communication performance as well as the static network performance than the Mesh networks (Miura et al., 2013; Punhani et al., 2014). However, the Torus network consumes much higher static power than Mesh networks. For example, 3D Torus interconnects

<table>
<thead>
<tr>
<th>MPC system</th>
<th>Performance (petaFlops)</th>
<th>Power (MW)</th>
<th>pFlops/MW</th>
<th>Interconnection Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sunway Taihulight</td>
<td>93.0</td>
<td>15.4</td>
<td>6.04</td>
<td>Sunway</td>
</tr>
<tr>
<td>Tianhe-2</td>
<td>33.9</td>
<td>17.8</td>
<td>1.91</td>
<td>Fat Tree Network</td>
</tr>
<tr>
<td>Piz Daint</td>
<td>19.6</td>
<td>2.27</td>
<td>8.63</td>
<td>Aries Interconnect</td>
</tr>
<tr>
<td>Gyoukou</td>
<td>19.1</td>
<td>1.35</td>
<td>14.14</td>
<td>Infiniband EDR</td>
</tr>
</tbody>
</table>
(used for Cray T3D) require 23.07% higher router power in comparison to 3D Mesh (used in MIT M-Machine) at the lowest level of a network with 64 nodes (Al Faisal et al., 2017). The power usage of MPC systems can be divided into two modules. One will be the on-chip module and another will be the off-chip module. Considering the on-chip module, an 80-tile teraFLOPS processor arranged as (8 x 10) 2D Mesh network with 65nm CMOS process requires 97W of electrical power (operating frequency was 4.27GHz) (Liu & Svensson, 1994) (Vangal, S. et al., 2008). In addition, 16-tile on-chip network requires about 36% of the total chip power (Wang & Peh, 2003). However, off-chip links also have a high impact on total power usage. For example, Infiniband QDR 40Gbps switch requires 1W of electrical power per link (NVIDIA, n.d.). On-chip network for supercomputers consists of a CPU core, on-chip level shared memory, and finally the router to connect neighboring cores through their router. Quriosity supercomputer ranked in Top500 (Supercomputer, n.d.), requires about 15km of wiring and also needs 600 kilowatts of electric power (BASF Supercomputer, n.d.). Finally, this research paper is immensely important for the field of interconnection networks due to the design consideration of on-chip as well as off-chip networks based on for conventional networks like- Mesh and Torus, especially for the hierarchical networks where on-chip levels are often considered as high degree networks and off-chip networks are considered as low degree networks in order to reduce the power consumptions. For example, 3D-TTN network (Al Faisal et al., 2021) considers the 3D Torus network for its on-chip module and the 2D Torus network for its off-chip connectivity. Similarly, a latest hierarchical interconnection network specially designed for exascale supercomputers named as Hierarchical Flattened Butterfly Network (HFBN) considers similar to 2D flattened butterfly architecture at the NoC level and the upper level is designed with 2D Torus network (Faisal et al., 2022). Hence, investigating the network performance with respect to latency and power usage are highly important for the field of interconnection networks.

ARCHITECTURE OF MESH AND TORUS NETWORKS

The modern interconnection networks of the MPC systems mainly focus on the fixed router radix because it is very important to maintain fixed router cost with the increased scalability. Increased router radix has the performance efficiency but also increases the router cost and also the power usages for the increased link connectivity and router activity. On the other hand, a constant router radix network helps to construct very large networks from the lowest network module. This regularity and modularity ensures that direct networks are often considered for the MPC systems. Table 2 shows the several topologies that are considered for various MPC systems. Mesh and Torus networks are the most common networks that have been adopted by supercomputers. Even one of the modern supercomputers like- Sunway TaihuLight can achieve 93PFLOPS with a power efficiency of 6.051
GFLOPS/watt used 2D Mesh interconnects (Fu, 2016). The main problem of those networks is the ill-conceived numbers of off-chip links. Those conventional networks are vastly used due to their network simplicity and reduced networks wiring complexity.

Mesh (Miura et al., 2013) is one of the k-ary n-cube networks, is one of the well-known networks in the field of interconnection networks, which is easy to layout because of its regular and equal-length links. Mesh network has been used in Tilera 100-core CMP. Moreover, hierarchical networks (Rahman & Horiguchi, 2005) like- TESH (Jain et al., 1997; Rahman et al., 2008) and 3D-TESH (Al Faisal et al., 2017) both used the 2D Mesh networks for their on-chip module. Fig. 1(a) shows the architectural interconnect for 2D Mesh. In addition, it has high path diversity, i.e., there are many ways to reach from one node to another. Along with the Mesh interconnection network for supercomputers, this network is also very popular for Wi-Fi systems, where multiple Wi-Fi devices act as a single Wi-Fi network.

Torus is also a k-ary n-cube network. However, the main difference between Mesh and Torus networks is the extra wrap-around links used by the Torus network. Mesh is not as symmetric on edges as the Torus network. Torus network doesn’t have this problem (Miura et al., 2013). It has a high bisection bandwidth than that of a Mesh network, and hence, it has high fault tolerance and path diversity. In contrast, it requires high cost, high power usage, and harder to layout on-chip and also requires unequal link lengths. Fig. 1(b) displays the interconnectivity of their nodes for a 3D Torus network. Similar to the TESH network, hierarchical networks like- TTN (Hafizur Rahman et al., 2013) and 3D-TTN (Al Faisal et al., 2016) used the 2D Torus and 3D Torus networks respectively at the on-chip module. Fig. 2 shows system cost with respect to chip-chip links (level-2 links) and

**Table 2. Commercially used networks in MPC systems**

<table>
<thead>
<tr>
<th>Supercomputers</th>
<th>Interconnection Networks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connection Machine CM-5 (Leiserson et al., 1996)</td>
<td>Fat-Tree</td>
</tr>
<tr>
<td>Intel iPSC-2 (Arlanskas, 1988; Nugent, 1988)</td>
<td>Hypercube</td>
</tr>
<tr>
<td>Intel Paragon (Intel Corp, 1991)</td>
<td>2DMesh</td>
</tr>
<tr>
<td>MIT J-Machine (Noakes &amp; Dally, 1990; Noakes et al., 1993)</td>
<td>3DMesh</td>
</tr>
<tr>
<td>K Computer (Ajima, 2018)</td>
<td>5/6DTorus</td>
</tr>
<tr>
<td>Sunway TaihuLight (Fu, 2016)</td>
<td>2DMesh</td>
</tr>
<tr>
<td>Cray T3E (Cray Research Inc, n.d.; Kessler &amp; Swarszmeier, 1993)</td>
<td>3DTorus</td>
</tr>
</tbody>
</table>

Figure 2. Static wiring cost analysis on the conventional networks

(a) Cost Analysis with 4K Cores [33]  
(b) Cost Analysis with 1M Cores
intra-rack links (level-3 links) (Fig. 2(a) is the cost for the 4096 cores and Fig. 2(b) is the scaled cost for 1M cores). This research considered the electrical links at the inter-chip level and optical links at the intra-rack level. The consideration for number of links has been shown at Table 3. This analysis explains that 2D Mesh network will require about 90.39% less amount of cost for designing level-2 and level-3 off-chip links than the 4D Torus network. On the other hand, fig. 3 shows the power usages for various network topologies with 4096 cores and 1M cores based on the static power usages. Here, 0.0135w is considered for each electrical interconnect at inter-chip level and 0.0101 w for each optical connections with 1.2w for each GBIC Module at the Intra-rack level connectivity.

**ROUTING ALGORITHM**

In this paper, the authors have considered deterministic dimension-order routing algorithm. In dimension-order routing each packet routes to each dimension until the distance of the dimension becomes zero, then it forwards packets to the next dimension. A packet starts its’ routing from the source node to the destination, though checking each dimension one by one. The authors consider the BookSim simulator (Jiang & Dally, 2013) for the evaluation of dynamic performance. Hence, this routing algorithm has been designed with the consideration of a simulator environment. This simulator requires the outgoing port number for each node routing path. Hence, when the routing algorithm is called, it returns the outgoing channel number to send the packet to the next node along the destination path. However, Mesh networks don’t have any wrap-around connection, hence no partition logic is being adopted for Mesh interconnection networks.

**Table 3. Total number links with 4K Cores**

<table>
<thead>
<tr>
<th>MPC system</th>
<th>No. of Inter-chip links</th>
<th>No. of Intra-rack links</th>
</tr>
</thead>
<tbody>
<tr>
<td>2DMesh</td>
<td>1536</td>
<td>384</td>
</tr>
<tr>
<td>2DTorus</td>
<td>1536</td>
<td>512</td>
</tr>
<tr>
<td>3DMesh</td>
<td>3840</td>
<td>1152</td>
</tr>
<tr>
<td>3DTorus</td>
<td>4864</td>
<td>1280</td>
</tr>
<tr>
<td>4DMesh</td>
<td>3840</td>
<td>4224</td>
</tr>
<tr>
<td>4DTorus</td>
<td>4864</td>
<td>5376</td>
</tr>
</tbody>
</table>

**Figure 3. Static Power analysis on the conventional networks**

(a) Power Analysis with 4K Cores       (b) Power Analysis with 1M Cores
This partition logic has been adopted for obtaining a better saturation rate for Torus networks. In the case of Mesh routing, the authors considered the default routing algorithm and Torus routing has been developed by our-self. However, this article has also shown some result analysis of default Torus routing. In the case of considering the routing algorithm for a Mesh network (Mesh_Routing()), where gN is defined by network dimension, gK is the total number of nodes in each dimension, cur is the current routing node number, gNodes is the total node number and dest is the destination node number. Dynamic routing algorithm (Torus_Routing()) is considered for the Torus routing. Our Torus routing algorithm considers less use of the wrap-around connection, which is the only difference between the default routing algorithms.

Mesh_Routing(int cur, int dest, int descending);
    if (cur = dest) then consume the packet; return 2 * gN; endif;
    if(descending), then
        for dim_left = gN - 1; dim_left > 0; --dim_left
            if((cur*gK/gNodes) != (dest*gK/gNodes)), then break; endif;
            cur = (cur * gK) % gNodes; dest = (dest * gK) % gNodes;
        endfor;
        cur = (cur * gK) / gNodes; dest = (dest * gK) / gNodes;
    endif;
    else, then
        for dim_left = 0; dim_left < (gN - 1); ++dim_left
            if ((cur % gK) != (dest % gK)), then break; endif;
            cur /= gK; dest /= gK;
        endfor;
        cur %= gK; dest %= gK;
    endelse;
    if (cur < dest), then return 2 * dim_left; endif;
    else, then return 2 * dim_left + 1; endelse;
end

Torus_Routing(int cur, int dest, int in_port, int *out_port, int *partition, bool balance = false);
    for dim_left = 0; dim_left < gN; ++dim_left
        if ((cur % gK) != (dest % gK)), then break; endif;
        cur /= gK; dest /= gK;
    endfor;
    if (dim_left < gN), then
        if (in_port/2 != dim_left), then
            cur %= gK; dest %= gK;
            diff = dest - cur; movedir = 0;
            if (diff > 0), then movedir = 0; endif;
            if (diff < 0), then movedir = 1; endif;
            if (movedir = 0 and diff > gK/2), then diff = diff-gK; endif;
            if (movedir = 1 and diff < -gK/2), then diff = diff+gK; endif;
            if (diff > 0), then *out_port = 2 * dim_left; dir = 0; endif;
            if (diff < 0), then *out_port = 2 * dim_left+1; dir = 1; endif;
            if (partition), then
                if ((dir = 0 and cur > dest) or (dir = 1 and cur < dest), then *partition = 1; endif;
                else, then *partition = 0; endelse;
            endif;
            else, then *out_port = in_port^{0x1}; endelse;
        endif;
    endif;
end
STATIC NETWORK PERFORMANCE ANALYSIS

The network topology holds the key to ensure the overall performance of the MPC systems. Interconnection networks are supposed to have low cost, low degree or radix, high connectivity, and low packet congestion. In this section, this paper would like to show the diameter performance and the average distance for the Mesh and Torus networks.

The diameter of a network should be small, which is the maximum inter-node distance between any distinct pair of nodes along its shortest path. A short distance will reduce the total message passing time. Hence, networks with small diameters are extremely desirable. The diameter of the 2D Mesh network can be calculated using equation 1 (where N is the number of nodes), whereas 2D Torus uses equation 2, and for k-ary n-cube networks require equation 3. Fig. 4 illustrates this diameter analysis of various networks, where the 5D Torus (5DT) network outperforms every other:

\[ \text{Diameter of 2D Mesh} = 2 \left( \left\lfloor \frac{N}{2} \right\rfloor - 1 \right) \] (1)

\[ \text{Diameter of 2D Torus} = \left\lfloor \frac{N}{2} \right\rfloor \] (2)

\[ \text{Diameter of k-ary n-cube} = \frac{nk}{2} \] (3)

Small diameter is preferable for networks however, considering only the diameter performance is not a good choice. This is due to the reason of a single node requires every other node rather than a single node. To mitigate this issue, a preferable choice is to consider the average distance, where the mean distance is calculated for all distinct pairs of nodes in a network. To calculate the average...

Figure 4. Diameter of various networks
distance of the 2D Mesh equation 4 is been used (where N is the number of nodes), equation 5 is used for 2D Torus and equation 6 is for k-ary n-cube networks. In short, fig. 5 shows the complete result analysis, where 5D Torus outperformed every other due to its high node degree (10):

\[
\text{Av. Dist. of 2D Mesh} = \frac{2}{3} \left( N^{1/2} \right)
\]

(4)

\[
\text{Av. Dist. of 2D Torus} = \frac{1}{2} \left( N^{1/3} \right)
\]

(5)

\[
\text{Av. Dist. of k-ary n-cube} = \frac{nk}{4}
\]

(6)

**DYNAMIC COMMUNICATION PERFORMANCE ANALYSIS**

The performance of supercomputers heavily depends on the network latency and its throughput (Nakao et al., 2020). Low network latency and throughput are not desirable at all. However, the performance of various networks also depends on the virtual channels and the number of router buffers. In this section, the authors like to evaluate the dynamic communication performance of Mesh and Torus networks through the cycle-accurate BookSim network simulator (Jiang & Dally, 2013) using only two virtual channels. Latency is defined as the time period that is required from the instance of a packet to the last flit of the message is received at the destination node. However, the network throughput is defined as the packet transmission rate for a specific traffic pattern. Table 4 depicts the simulation environments for the dynamic performance analysis.

Figure 5. Average distance of various networks
Table 4. Simulation condition for dynamic performance analysis

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traffic Patterns</td>
<td>Uniform and Non-uniforms</td>
<td>-</td>
</tr>
<tr>
<td>Number of Nodes</td>
<td>4096/1024</td>
<td>Processing Nodes</td>
</tr>
<tr>
<td>Message Size</td>
<td>128</td>
<td>Bits</td>
</tr>
<tr>
<td>Flow Control</td>
<td>Wormhole</td>
<td>-</td>
</tr>
<tr>
<td>Buffer size</td>
<td>8</td>
<td>Flits</td>
</tr>
<tr>
<td>Simulation Cycle</td>
<td>5000</td>
<td>Clock Cycles</td>
</tr>
<tr>
<td>Virtual Channels</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>Packet Size</td>
<td>16</td>
<td>Flits</td>
</tr>
</tbody>
</table>

Uniform Traffic Pattern

Uniform traffic pattern is defined as the randomly selected source and destination node for each generated message. Hence, each node sends a message to another node with an equal probability. Fig. 6 portrays the dynamic performance analysis for Mesh and Torus networks under uniform traffic patterns. This figure ensures that 2D Mesh and 2D Torus network shows the worst performance by comparing it to 3D Mesh, 3D Torus, 4D Mesh/Torus, and 5D Mesh/Torus networks. The zero load latency of Mesh networks is worse than the Torus network. However, the saturation latency of a Mesh network is better than the Torus networks. This figure shows the performance analysis of BookSim default Torus network routing (2DT(4096)D, 3DT(4096)D, 4DT(4096)D) which ensures that our algorithm shows a little better performance in case of zero load latency. However, the default algorithm shows better saturation load latency than algorithm 2. The important finding from this figure is the zero load difference between the various networks; 3D, 4D, and 5D Mesh/Torus networks show the very margin-able differences between them. In contrast, zero load latency of 2D Mesh/Torus is completely undesirable for MPC systems.
Transpose Traffic Pattern

Transpose traffic pattern transmits the packets to fixed source-destination pair. For example, node number $a_0$ will transmit the packet to $a_n^2$, where $n$ is the total node number. Fig. 7 shows the transpose traffic analysis for Mesh and Torus networks. This figure also ensures that Torus networks show much better performance than the Mesh network in case of zero load latency. In contrast to uniform traffic, this pattern shows better saturation load performance for Torus networks over the Mesh networks even with low virtual channels. This figure also confirms the worst performance for 2D Mesh/Torus networks. However, interestingly, 2D Torus network shows a better saturation rate than the 3D Mesh & 4D Mesh/Torus networks.

Perfect Shuffle Traffic Pattern

Perfect shuffle traffic pattern transmits a packet to the fixed selected source and destination node for each generated message. The choice of source and the destination node is based on the rotation of the left 1 bit. Fig. 8 shows the perfect shuffle traffic performance analysis for

![Figure 7. Transpose traffic of various networks](image)

![Figure 8. Perfect shuffle traffic of various networks](image)
conventional networks. This traffic pattern shows the exact opposite trend from the other two traffic patterns, where this figure ensures the superiority of Mesh networks over the Torus networks in case of zero load latency and saturation load latency. However, the performance of 2D networks are usual as before and the others show a very narrow difference between them. Hence, the supercomputer, which is designed with a Torus network, must not use a perfect shuffle for running various applications.

**Bit-Reverse Traffic Pattern**

Bit-reverse traffic pattern sends the packets with a source address of \( a_0 \) to destination node \( a_{(n-1)} \) (fixed pair). Fig. 9 shows the traffic analysis for the bit-reverse traffic patterns. This traffic pattern is very useful for a low number of nodes. It ensures better performance with a low number of nodes, especially, for the saturation load. For example- 5D network with low nodes can tolerate heavy traffic loads finally before getting saturated. However, other than 2D Torus network, the rest of the 3D, 4D, and even 5D Torus networks show worst performance than the Mesh networks in case of saturation load.

**ESTIMATION OF POWER CONSUMPTION**

With modern advancements, the biggest concern for supercomputers is power dissipation. Modern supercomputer like- Sunway System has achieved about 93 PFLOPS performance. To achieve this performance Sunway system requires about 15.3MW electrical power installed with 2D Mesh network (Fu, 2016). This section will explain the effect of on-chip power usages on the high degree Mesh and Torus networks.

**Assumptions for Power Model**

Power consumption at the on-chip network level is up to 50% of total chip power usage (Liu & Svensson, 1994) due to a large number of on-chip links in comparing less numbered of off-chip links. Hence, we have considered only the on-chip power estimation for various networks. The power consumption for this paper considers on-chip network simulation along with the tabular based default routing of GARNET network simulator (Agarwal et al., 2009) and the authors have estimated the static and dynamic power for the links as well as for the routers. Therefore, at the on-chip level, the authors had to take account of every interconnected link.

![Figure 9. Bit-reverse traffic of various networks](image-url)
On-Chip Power Model

Orion energy model (Kahng et al., 2011) has been considered as the on-chip power model in this paper using 32nm fabrication process for various networks. This consideration leads to the evaluation of the static and dynamic power usage for the routers and the inter-router links. However, for analyzing various networks, this paper has used the GARNET network simulator (Agarwal et al., 2009) along with the Orion energy model. To evaluate the power dissipation for various networks, dynamic power and leakage power are the main sources of power consumption. Hence, the authors have analyzed both dynamic and leakage power for the routers and interconnected links. Router total energy depends on energy consumption by the total activity at the local & global arbiters, the read \(E_{br}\) and write \(E_{bw}\) to router buffers, and finally for the total number of crossbar traversals \(E_{xb}\). Equation 7 shows the router’s total energy consumption (Kahng et al., 2011). The dynamic energy is defined in the Orion power model as equation 8, where \(\alpha\) is the switching activity, \(C\) is the capacitance and \(V\) is the supply voltage (Kahng et al., 2011):

\[
E_{\text{router}} = E_{\text{buffer\_write}} + E_{\text{buffer\_read}} + E_{\text{sw\_arb}} + E_{\text{wb\_arb}} + E_{\text{xb}}
\]  

\[
E = 0.5\alpha CV^2
\]

Power Consumption for Mesh and Torus Networks

In January 2011, Samsung developed a 30nm ~ 39nm fabricated processor module, which can obtain a data transfer rate is about 2.133 Gbit/s with the supply voltage of 1.2V (Intel, n.d.). Hence, our consideration for the clock frequency with 2.133 GHz, supply voltage 1.2V, and uniform traffic pattern with 2.5mm per link length. Table 5 shows the simulation condition of the on-chip networks. Those simulations show the various cases of power usages with traffic loads from 0.0015 to 0.0065. Though the increasing traffic loads don’t have any effect on the leakage power usage, it highly affects the dynamic power usage. Fig. 10 shows the link power dissipation of various networks in considering the 64 numbers of nodes for 2D and 3D Mesh/Torus networks, 256 nodes for 4D Torus, and 512 nodes for 5D Torus. Fig. 11 shows the router power dissipation including the router leakage power, router dynamic power, and the clock power considering 64 routers for every network. Fig. 10 and Fig. 11 consider the traffic load as 0.0015 flits/second. However, Fig. 12 (same nodes like Fig. 10) and Fig.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fabrication Process</td>
<td>32nm</td>
<td>-</td>
</tr>
<tr>
<td>Link Length</td>
<td>2.50</td>
<td>[mm]</td>
</tr>
<tr>
<td>Operating freq.</td>
<td>2.133 (\times) 10^9</td>
<td>Hz</td>
</tr>
<tr>
<td>Transistor Type</td>
<td>NVT</td>
<td>-</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2</td>
<td>volt</td>
</tr>
<tr>
<td>Traffic Pattern</td>
<td>Uniform Traffic</td>
<td>-</td>
</tr>
<tr>
<td>Message inject rate</td>
<td>0.0015 - 0.0065</td>
<td>flits/cycle/node</td>
</tr>
<tr>
<td>Message size</td>
<td>128</td>
<td>bits</td>
</tr>
<tr>
<td>Simulation Cycle</td>
<td>5000</td>
<td>Clock Cycles</td>
</tr>
<tr>
<td>Virtual Channels</td>
<td>2</td>
<td>-</td>
</tr>
</tbody>
</table>
13 (same number of routers like Fig. 11) show the traffic load as 0.0065 flits/second. Fig. 10 and Fig. 12 show that the 3D Mesh/Torus networks require higher link power usage than the 2D Mesh/Torus networks. In Fig. 12, the static power remained the same, but dynamic power was changed in comparison with Fig. 10 and 3DT requires less dynamic power than the 2D networks. On the other hand, in the case of router power dissipation obtained from Fig. 11 and Fig. 12, show that Torus networks require higher power usage than the Mesh networks and clock power requires a high portion of amounts in considering the total power usage. Even though there is a change in traffic loads in Fig. 13, static power and clock power remain the same as Fig. 11. Router power analysis shows that high degree networks consume much larger power than low degree networks.
EFFECTS OF VIRTUAL CHANNELS

Virtual channels are the key to solve the deadlock avoidance problem in any interconnection networks. Moreover, virtual channels help to increase the network throughput as well as the network latency. Suppose, a single router received two different packets ($P_0$, $P_1$) from two different source nodes, and expected to forward those packets through the same physical link. In such cases, one of them could block the whole physical link until his transmission is over. However, using the virtual channels both packets could move forward with half speed on a flit-by-flit approach. Hence, the MPC systems must consider the number of virtual channels to make their network deadlock-free. For instance, the
BlueGene/L supercomputer uses 4 virtual channels for its deadlock-free routing in the network (IBM Blue Gene 100, n.d.). Out of these four, two of them are used for the deterministic routing and the rest two virtual channels are used for the adaptive routing. In this section, the authors have investigated the effects of using high virtual channels in 3D Mesh/Torus networks with respect to packet latency and router level power usage. The simulation environments and parameters for Table 6, is similar to Table 4 with 4096 nodes and uniform traffic pattern. However, here the paper considered only zero load latency (0.0015 flits/cycle) as the injection rate. Table 6 shows the average packet latency for zero traffic loads with 3D Mesh/Torus networks using 2 and 4 virtual channels. This result illustrates that the Mesh network yields the worst performance in both cases. On the other hand, Table 7 shows the power estimation for two and four virtual channels based on the simulation considerations of Table 5 and 64 nodes only. This analysis shows that with changes in virtual channels, router static power is highly affected. However, router clock power and dynamic power have no impact or very little impact. Hence, the consideration of a suitable number of virtual channels is also important for reducing the total power usage of the MPC systems.

**DISCUSSION**

The main contribution for this research was to investigate the power and performance analysis of high dimensional Mesh and Torus Networks. Moreover, the authors had also investigated the effects of virtual channels on Mesh and Torus Networks with respect to three-dimensional Mesh and Torus Networks. It is obvious that high degree networks like three-dimensional or four-dimensional Mesh/Torus networks will show high saturation rate, better network latency than two-dimensional Mesh/Torus networks. However, power usage for two-dimensional Mesh/Torus networks is less than other high dimensional networks. For example, 2D Mesh network requires about 24.22% less router power usage than the 3D Mesh network. On the other hand, considering only 2 virtual channels, the saturation rate of the Torus is faster than the Mesh network. However, increasing the number of virtual channels to four, the Torus network shows much better saturation rate than the Mesh networks. Even the Mesh network shows the slightly poor zero load latency with four virtual channels than the two virtual channels, which is about a 0.04% decrease in clock cycles. In the case of two virtual channels, the difference of clock cycles at zero load latency between 3D Mesh and 3D Torus is about 7.03% less.

<table>
<thead>
<tr>
<th>Networks</th>
<th>Packet Latency with 2VC (clock cycles)</th>
<th>Packet Latency with 4VC (clock cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3DMesh</td>
<td>103.97</td>
<td>104.01</td>
</tr>
<tr>
<td>3DTorus</td>
<td>96.66</td>
<td>95.51</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Networks</th>
<th>Router Dynamic Power (Watt)</th>
<th>Router Static Power (Watt)</th>
<th>Router Clock Power (Watt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3DMesh (2 VC)</td>
<td>0.16</td>
<td>8.92</td>
<td>7.07</td>
</tr>
<tr>
<td>3DTorus (2 VC)</td>
<td>0.17</td>
<td>12.52</td>
<td>8.70</td>
</tr>
<tr>
<td>3DMesh (4 VC)</td>
<td>0.18</td>
<td>27.96</td>
<td>7.07</td>
</tr>
<tr>
<td>3DTorus (4 VC)</td>
<td>0.19</td>
<td>44.69</td>
<td>8.70</td>
</tr>
</tbody>
</table>
CONCLUSION

In this research plan, the authors have analyzed the network performance for Mesh and Torus networks with the parameters like-diameter and average distance for investigating the static network performance, and also the network latency for investigating the dynamic network performance. Regarding the performance concern, this paper was able to show that 3D Torus can achieve about 57.07% better dynamic communication performance than 2D Torus network and 4D Torus can show about 25.95% better performance than 3D Torus network considering the zero load latency in the uniform traffic pattern. Moreover, the saturation rate for low degree networks is much faster than the high degree networks. In the case of power analysis on Mesh and Torus considering the link’s and router’s static as well as dynamic power usage, the authors could able to show that 2D Mesh network requires about 24.22% less router power usage than the 3D Mesh network and 5D Torus requires about 66.8% higher router power usage than the 3D Torus network with 0.0015flits/cycle traffic load. However, in considering the 0.0065flits/cycle traffic load 5D Torus network requires about 67.31% higher router power usage than the 3D Torus network. This analysis ensures that high degree networks will require huge power usage even at the on-chip level. Furthermore, in the case analyzing the effects of virtual channels on Mesh and Torus networks, the difference of clock cycles at zero load latency between 3D Mesh and 3D Torus is about is about 8.17% lower with four virtual channels. On the other hand, in case of power usage in router static power has been significantly increases with the increase of virtual channels. For example, in case of 3D Torus network, 2 VCs require 71.98% less static power than 4 VCs. Hence, the proper choice of required number of virtual channels is very important for network performance as well as for power usages.

COMPETING INTERESTS

The authors of this publication declare there is no conflict of interest.

FUNDING AGENCY

This work wasn’t supported by any funding agency.
REFERENCES


Faiz Al Faisal received his B.Sc. degree in Computer Science and Engineering from Khulna University of Engineering and Technology (KUET), Khulna, Bangladesh, in 2009. He received his M.Sc. degree in Information Science from Japan Advanced Institute of Science and Technology (JAIST), Japan, in 2015. He has also persuaded a doctoral degree in Information Science from JAIST in 2018. Currently, Dr. Faisal is working as an assistant professor in the Dept. of Computer Science and Engineering (CSE) at Green University of Bangladesh (GUB), Dhaka, Bangladesh. Before joining GUB, he worked as an assistant professor in the Canadian University of Bangladesh (CUB) and North South University (NSU), Dhaka, Bangladesh. Prior to his M.Sc. graduation, he served as an IN-VAS associate Engineer at Orascom Telecom Bangladesh Limited in 2010-2013. He was also provisioned as a software engineer at Leads Corporation Limited, Bangladesh, in 2009. His current research interest has been centered on parallel computer systems, interconnection networks, and machine learning algorithms.

M.M. Hafizur Rahman received his B.Sc. degree in EEE from KUET, Khulna, Bangladesh, in 1996. He received his M.Sc. and Ph.D. degrees in Information Science from the JAIST in 2003 and 2006, respectively. Dr. Rahman is currently working as an assistant professor in the Dept. of CN, CCSIT, KFU, Saudi Arabia. Prior to join in the KFU, he was assistant professor in the Xiamen University, Malaysia & IIUM, Malaysia and associate professor in the CSE, KUET, Khulna, Bangladesh. He was also a visiting researcher in the School of Information Science at JAIST and a JSPS postdoctoral research fellow at Graduate School of Information Science (GSIS), Tohoku University, Japan & Center for Information Science, JAIST, Japan in 2008 and 2009 & 2010-2011, respectively. His current research interests include hierarchical interconnection networks and optical switching network, software defined network

Yasushi Inoguchi received his B.E. degree from Department of Mechanical Engineering, Tohoku University in 1991, and received MS degree and Ph.D from JAIST (Japan Advanced Institute of Science and Technology) in 1994 and 1997, respectively. He is a Professor of Research Center for Advanced Computing Infrastructure, JAIST. He was a research fellow of the Japan Society for the Promotion of Science from 1994 to 1997. From 2002 to 2006 he was a researcher of PRESTO program of Japan Science and Technology Agency. From 2008 to 2009 he was a courtesy senior research scholar at University of South Florida. His research interest has been mainly concerned with parallel computer architecture, interconnection networks, GRID/Cloud architecture, and high performance computing on parallel machines. Dr. Inoguchi is a member of IEEE, IEICE & IPS of Japan.