Chapter 2

Low Power Strategies for beyond Moore’s Law Era:
Low Power Device Technologies and Materials

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ABSTRACT

Semiconductor industries are facing a lot of problems in designing the chips consist of transistors with less than 10nm technology. Moore’s law which predicted the scaling down of semiconductor devices has forced the researchers to look upon the devices in another aspect. So, various architectures and materials are invented to increase the reliability, speed and most importantly low power operation without increasing the size of devices. The on-set of nanotechnology and nano-science leads to unconventional 3D structure devices to and 0-dimensional structures. This chapter gives a general overview of the various technologies; materials and architectures researchers are concentrating to continue the technology beyond Moore’s law with low power consumption.

1. INTRODUCTION

Moore’s law: It is the observation by Gordon Moore that the number of transistors in a square inch area for the integrated circuits had doubled every year. But in subsequent years, this enhancement of density has slowed down i.e. doubling in two years but still it will be continue living for another some years.

Traditionally, the MOSFETs are designed in planar structure form to design the integrated circuits ICs. With the down scaling of transistor sizes beyond 45nm technology, introduction of short channel effects come into consideration. This effect hence introduces leakage current which increases the power

consumption even at the zero operation state. Also passive power dissipation and non uniformity in device structures and doping concentrations are faced by the fabrication members. These problems are somewhat solved in considerable amount by introduction of multi-gate structure which is explained in below section.

**Background**

Researchers are also going for various architectures which are something different from present designs of transistors. These new architectures are found to be very good in achieving the most important specifications especially low power implementation of devices in various circuits. Also, silicon on insulator based technologies; materials having high k-dielectric are also source of achieving some of the design constraints like low scaled devices and low power.

With the more demanding of low power as well as compact size devices in market makes the researchers to think more out of box ideas in order to compensate the demands. These ideas strengthen Moore’s law to get extended for further some decades as the size of transistors has to be minimized beyond the optimized level taking silicon as major ingredient of semiconductor. So, different materials exhibiting nearly semiconductor properties especially lower band-gap property have been the source of replacement for the silicon based gates of transistors. Not only that to miniaturize the device and hence the integrated circuits, researchers opted for reducing dimensionality of the devices which can helpful for miniaturizing them.

In this chapter, there is a general overview of various types of modified devices in structures, materials and miniaturizing the dimensions of the semiconductor materials.

**2. LIST OF LOW POWER DEVICES**

**2.1 Floating Gate MOSFET**

It is a type of Metal Oxide Semiconductor Field Effect Transistor where gate is electrically isolated. A number of secondary gates are deposited over the isolated floating gate. This isolated gate is surrounded by highly resistive material and hence charge stored inside it can be retained for a longer period of time. As the construction suggests it can be a building block of various flash memories like EPROM, EEPROM. Also it has other applications in designing digital potentiometers, neural network constitutional elements and also digital to analog converters (DACs) as mentioned by Holer et al. (1989). When implemented various computational circuits instead of traditional MOSFETs, the average power was found to be less as it reduces the leakage currents especially during the OFF state as it stores charge.

This type of transistor was first made by Kahng and Sze in 1967 to store data. But it has some drawbacks of low input transconductance and low output resistance.

Implementation of FGMOS allows threshold voltage ($V_{th}$) controllability without reducing the feature size, thus operates at power supply voltage levels which are well below the intended operational limit was shown by Thomsen & Brooke (1991). A typical multi-input floating gate transistor is shown in Figure 1. It is a conventional MOSFET in which the gate is capacitively coupled to the input using another polysilicon layer. FGMOS device provides impressive features relevant to low-voltage, low-power context.
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