Chapter 3

Challenges and Limitations of Low Power Techniques:
Low Power Methodologies in Analog and Digital Circuits

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ABSTRACT

In contemporary world the technology has kept its vast identity in developing ultra NANO devices to give up the compact device utilities, in VLSI, Metal Oxide Semiconductor device plays an key role in power dissipation product, in terms of MOS theory characteristics it is predefined that a MOS transistor can conduct easily with low voltage which gives low power but in DSM technology there is a likelihood to achieve ultra low power, so this can be achieved due to the rapid shrinking of gate length, here the chapter deals with challenges and limitations of low power techniques. The predominant way to generate low power is to start with the fundamental principles that are defined in the existing technologies that it gives low power with less leakage current. Apart from this parameter consideration is also required to achieve this. The successful and the major parameter in generating low power is that the shrinking of supply voltage. To go through this, upcoming sections gives the brief idea about the different techniques that are utilized to generate low power with less leakage.

INTRODUCTION

VLSI is the domain, dealing with MOS transistors, according to the principle given by scientist Moore’s the count of the transistors on printed circuit board has doubled for every 18 months as this got influenced the engineers to develop Compaq board. On the other hand circuit logic and managing power was the main focused to enhance the technology. So there after change in the technology has forced the device

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developers to manufacture and operate with ultra low power. Here the chapter looks forward with why low power, techniques that achieve low power, limitations and challenges.

Before dealing with low power techniques, let us know why power has become the major parameter in VLSI, as it is the collaboration of MOSFET devices, due to its characteristics properties it has the feather of conducting with less power, taking this in to account design engineers has contributed the work with several techniques to achieve ultra low power. Due to the rapid growth in technology, power become the main concern parameter for every operating system because now a days we are surviving with smart technology before this came into existence few decades ago power dissipation was the major issue rather than the power consumption because as now we have a high end technology resources which are further developed for upcoming technologies.

BACKGROUND

This chapter deals with the brief description of the challenges facing by the present semiconductor industries and researchers. There are many techniques implemented to improve analog and digital circuits which can enhance the reduction of power consumption as well as leakage current. Another crucial driving factor is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems.

WHY LOW POWER?

Digital integrated circuits are the motivating source in VLSI for innovating performance of various applications like computing and other digitized simulation, related to technology and science. The insist for digital integrated circuits will persist to enhance in near future, due to its some of the salient features like low power, reliable performance and improvements in the processing technology.

According to Moore’s law, the prediction in development of integrated circuits has various interpretations such as the density of devices gets incremented to ten folds for every seven years. So the need of low power got arises for such progression forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz.

While the transistor count got doubled as years go by, therefore the power dissipation increases exponentially, because of ever-shrinking size of integrated circuits, such power incrimination introduces a reliability concern such as electro migration and hot carrier induced device degradation, resulting in the loss of performance. The most convenient way to diminish the power consumption of digital circuits is finite reduction in supply voltage, in fact the average power consumption of CMOS circuits is proportional to the square of the supply voltage, and on other hand electric field should also be maintained at acceptable level. To ensure performance loss can be conquer for standard CMOS technologies by introducing more parallelism is shown and authors discusses about the research done in Veendrick (1984), Rabaey (2002), Horowitz, et.al (1994), and/or to modify the process and optimize it for low voltage operation is given in Horowitz, et.al. (1994), Sakurai (1990), Chandrakasan (1995).
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