Chapter 7

State-of-the-Art Master Slave Flip-Flop Designs for Low Power VLSI Systems

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ABSTRACT

This chapter presents a comprehensive overview of the conventional fully static master slave flip-flops used in low power VLSI systems where power budget is critical. In addition, the chapter also presents alternative realization of fully static master-slave flip-flops utilizing a modified feedback strategy. The flip-flops designed on the basis of modified architecture have been explained in detail and compared with state-of-the-art master slave flip-flop designs available in the literature. Extensive capacitance calculations have been performed in terms of clock load and capacitance at internal nodes has also been estimated for all the flip-flop configurations. This is executed in order to compare their relative power and delay characteristics which are well supported by simulation results.

INTRODUCTION

Major technological advancements in low power domain during the last decade have been associated with phenomenal demand for portable electronic devices. Flip-flops (FFs) and latches are considered as indispensable components for design of synchronous digital VLSI systems. The maximum operating speed of clocked digital systems is determined by the FFs. From a low power design perspective, nearly 30 - 70% of the total chip power dissipation is due to FFs and the clock distribution network (Yeap, 1998; Kawaguchi & Sakurai, 1998). Reducing the clock power of FFs is thus a serious bottleneck for digital IC
designers. Various attempts have been reported in the past to reduce the clock load and associated power dissipation in the clocking network (Oklobdizija, Stojanovic, Markovic, & Nedovic, 2003; Giacomotto, Nedovic, & Oklobdizija, 2007; Mesgarzadeh, Hanson, & Alvandpour, 2007). Moreover, a design with a high transistor count occupies larger area on chip and leads to an increase in the overall manufacturing cost. Hence, it has always been a challenge to explore more efficient FF designs in terms of enhanced speed, reduced power dissipation and minimum transistor count.

FFs are broadly classified into the following four major categories depending on the type of application viz:

- Master-slave FFs
- Pulse triggered FFs (implicit pulse triggered and explicit pulse triggered)
- Differential FFs
- Dual-edge triggered FFs (Alioto, Consoli, & Palumbo, 2015; Alioto, Consoli, & Palumbo, 2011b).

Master-slave FFs are generally utilized for low power systems whereas pulse triggered FFs find their use in high speed applications. Differential FFs are most suitable for deeply pipelined systems where the FF must supply complementary output signals to the subsequent logic. As a consequence, both the outputs need to be generated at the same time to improve performance by equalizing worst case delays (Myjak, Frias, & Jeon, 2006; Nikolic et al., 2000). On the other hand, a double edge triggered flip-flop (DETTFF) is useful for maintaining a constant throughput while operating at only half the clock frequency.

Master-slave FFs are further classified into non-clock gated FF structures and clock-gated topologies as shown in Figure 1. Amongst the non-clock gated FFs, Transmission gate flip-flop (TGFF) represents the most efficient design in terms of power-delay product (PDP) (Consoli, Palumbo, Rabae, & Alioto, 2014; Alioto, Consoli, & Palumbo, 2010) while modified C-MOS based flip-flop (mC-MOSff) (Chao & Johnston, 1989) is considered to be area efficient. Write port master-slave FF (WPMS) (Markovic, Tschanz, & De, 2003) and pass transistor logic style FF (PTLFF) (Hossain, Wronski, & Albicki, 1994) show degraded power-delay tradeoff characteristics. This is due to adoption of NMOS pass transistors in the critical path and presence of partially non-gated keepers. Gated master-slave latch (GMSL) (Strollo, Napoli, & Caro, 2001) and Data-transition lookahead FF (DTLA) (Nogawa & Ohtomo, 1998) represent the FFs belonging to the clock-gated class. However, the obvious limitation of clock gated FFs in terms of enhanced delays and increased area overhead, restricts their use to applications where power budget is critical and input switching probability is sufficiently low (Strollo & Caro, 2000). In this chapter, an alternative design approach for both types of master-slave FFs viz. TGFF and mC-MOSff has also been introduced based on a new architecture with reduced transistor count while simultaneous improvements are obtained in power-delay-area product (PDAP). The proposed configurations modified transmission gate FF (MTGFF), hybrid master-slave FF (HMSFF), mC-MOSff1 and mC-MOSff2 fall under the non-clock gated FF category.

This chapter is organized as follows. Section 1.2 explains the basic building blocks of sequential digital systems. Section 1.3 differentiates between dynamic and static latches and FFs. Section 1.4 presents a comprehensive review of conventional FF design techniques and introduces a novel architecture for the design of master-slave FFs. Based on this architecture, four new FF circuits have been implemented viz. MTGFF, HMSFF, mC-MOSff1 and mC-MOSff2 (Singh, Tiwari, & Gupta, 2014). Section 1.5 describes the simulation parameters and test bench used for executing this work. Section 1.6 illustrates the simula-
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