Chapter 10
Low Power Arithmetic Circuit Design for Multimedia Applications

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ABSTRACT

The objective of this chapter is to describe the various designed arithmetic circuit for an application of multimedia circuit that can be used in a high-performance or mobile microprocessor with a particular set of optimisation criteria. The aim of this chapter is to describe the design method of binary arithmetic especially using by CMOS and Pass Transistor Logic technique. The pass transistor techniques are reduced the noise margin for small circuit, which can be explained in this chapter. This chapter further describe the types of arithmetic and its techniques. The technique design principle procedure should make the following decisions: circuit family (complementary static CMOS, pass-transistor, or Shannon Theorem based); type of arithmetic to be used. The decisions on the designed logic level significantly affect the propagation delay, area and power dissipation.

1. INTRODUCTION

Reductions in power dissipation and improvements in speed require optimisation at all levels of the logic design. The proper circuit style and methodology are important factors to be considered for low power design. High-speed computation is now the expected norm for the average user. Likewise, another significant change in user attitudes is the desire to access computation from any location, without physically connecting to a wired network. According to Swaroop Ghosh, Kaushik Roy (2008), the requirement of portability thus places severe restrictions on size, weight, and power. The power is particularly important since absolute battery technology only provides 20 W-hrs of energy for each pound of weight. Improvements in battery technology are being made, but it is unlikely that a dramatic solution to the power problem is forthcoming. It is projected that only a 30% improvement in battery performance will

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be obtained over the next 5 years. Different circuit design techniques must be considered in order to maximise efficiency in terms of speed and power dissipation.

The increasing demand for low-power Very Large Scale Integration (VLSI) can be addressed at different design levels, including the architectural level, circuit layout, and the process technology level. At the circuit level, there is considerable potential for power savings by means of proper choice of a logic style for implementing combinational circuits. Marios Psilogeorgopoulos (1999) determine, all the important parameters governing power dissipation, switching capacitance, transition activity and short-circuit currents are strongly influenced by the chosen logic style. The low-power logic styles reported in the literature have mainly focused on particular logic cells, namely, full adder, full subtractor, multiplier, divider, XOR, NAND, OR and AND gates. In this chapter, low power logic circuit investigations are extended to a much wider set of logic gates and to arbitrary combinational circuits. Actual logic gates designs are implemented into multiplier and divider circuit.

The power dissipation has become a critical design metric for an increasingly large number of VLSI circuits. Mohab Anis (2002), determine, the exploding market for portable electronic appliances fuels the demand for complex integrated systems that can be powered by lightweight batteries with long times between recharges. The goal of extending the battery lifespan of portable electronics can be achieved by reducing the energy expended per arithmetic operation, but low-power consumption need not necessarily imply low energy. A circuit can consume very low power by clocking at an extremely low frequency to execute an arithmetic operation, but it may then take a very long time to complete the operation. One of the objectives of the present work is to investigate the effect of reduced supply voltage on the optimal energy efficiency of the full adders designed with different logic styles based on Ultra Deep Sub Micron (UDSM) process technology. Several circuit design techniques are compared in terms of speed and power dissipation. All kind of circuits is to be implemented and design technique can be chosen depending on the applications. The designed circuit are given different performance, which become important and disallow the formulation of universal rules for optimal logic styles.

1.1 Need for Low Power

The demand of low power microelectronics can be traced to the invention of the transistor in 1947. According to Gunok Jung, (2005), the elimination of the crushing need for several watts of heater power and several hundred volts of anode voltage in vacuum tubes in exchange for transistor operation in the tens of mill watts range was a breakthrough of unparalleled importance in electronics. The motivation for low power electronics comes from two reasonably distinct sources:

1. The most recent need is for ever-increasing packing density in order to further enhance the speed of high performance systems. This, in turn, imposes severe restrictions on power dissipation density.
2. The broadest need is for conservation of power in desktop systems, where a competitive lifecycle cost-to-performance ratio demands low power operation to reduce power supply and cooling costs.

Marios Psilogeorgopoulos, (1999) found that high speed system and low power operation classes need to encompass a substantial majority of current applications of electronic equipment. Low power electronics has become mainstream in the effort to achieve Giant Scale Integration (GSI). As digital computer arithmetic is an aspect of logic design with the objective of developing appropriate algorithms in order to achieve an efficient utilisation of the available hardware. The hardware can only perform a
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