Chapter 11
Case Study:
System on a Chip for Electric Stimulation

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ABSTRACT

Integrated circuits have been predominantly designed and developed by large firms and manufacturers; nowadays, any electronic engineer should be able to develop specific and innovative low-power designs using available open cores. This chapter presents the design process for a specific chip, beginning with a definition of its function, design considerations, power analysis, performance optimization, and chip optimization. The hardware and software for this circuit were developed for low-power implementation: it includes a processor, memory blocks, ports, buses, and a proposed application program, so it can be used as a starting point for other low-power very-large-scale integration (VLSI) circuits. The chip uses frequency synthesis and configuration parameters to deliver electric signals on a variety of waveforms and patterns. This design can be used in many research fields and application areas, where experiments or portable devices need low-power, programmable, and configurable electric signal generators.

INTRODUCTION

This system on a chip (SoC), developed by the author, is based on open cores and uses DDFS (direct digital frequency synthesis) algorithms. It is intended to operate as a standalone module or to interconnect with other devices or processors. It has been presented in medicine and biology forums (Lopez et al., 2011), and it has been used in scientific instruments (Lopez et al., 2013).

This SoC uses an OR1200 processor (Open RISC 1200), program memory, data memory, external address bus, data bus, communication port, interrupt controller, clock, reset, and general purpose input/output (GPIO) ports. All of its hardware cores are open source. The application program is proposed and optimized for minimum power and memory access. At the end of this chapter, an analysis of possible applications is presented, where this SoC can be used with little or no modifications.

A processor based SoC was selected over a gate-level design for several reasons: a different application program can be developed and uploaded with no modifications on the hardware design, the modular

design allow upgrading the processors or extending the memory easily, additional cores and functionality can be added thanks to the modular design, and it still is a specific application design while keeping the openness of a configurable and programmable system.

Throughout the entire design process, a low-power goal was pursued, both from a hardware and software perspective, as this integrated circuit is intended for embedded and portable systems.

The developed SoC has an area of 4.03 mm$^2$, 189 pins, an operating frequency of 180 MHz, and a power consumption of 0.52 watts when fabricated on 180 nm technologies. The design flow is explained, showing calculations for every design stage. The flow covers the synthesis process, area optimization, power calculations, performance optimization, IO ring definition, and place and route procedure.

As for the application program, the implemented methodology that is used to generate and deliver electric signals is presented, comparing a memory-intensive methodology versus a computation-intensive methodology. A selection of signal parameters and patterns is defined in order to ensure that a wide variety of applications is covered by this design. Waveforms (square, triangle, sine, and saw tooth) can be simultaneously delivered in separate output channels, or they can also be superimposed in one output channel.

A simple user interface is developed, so anyone can use this system without needing to understand the integrated circuit theory or the frequency synthesis methodology. The chip is developed featuring a modular design, so cores can be updated or upgraded using new releases. Similarly, application areas not currently covered can be achieved with small modifications to this design.

This system can be used as an example to develop other systems, and also can be used in other applications such as particle manipulation, pollution detection, water and food quality, cell detection, nano-manipulation, and biomedical analysis. Generally speaking, any application that needs electric signals on different waveforms, frequencies and patterns, can use this system.

**Background**

This chapter reviews the design flow for an application-specific integrated circuit that can be easily customized for other applications. Design parameters such as power, area, and performance are presented through several optimization rounds (Lopez et al., 2011). Open cores are used throughout the entire design, so no licensed circuits are needed. The design tradeoffs are presented, and a practical case with its actual numbers and results are exposed. This integrated circuit is used as an example on how to design your own SoC or a scientific instrument (Lopez et al., 2013) using open cores (OpenCores, 2014) and CAD tools (Jupiter, 2006) to achieve a low-power system. This chapter presents the definition of this system, as well as its design flow and implementation. Previous related works have been published, but they lack one or more of the following characteristics: SoC and labs on chip that are not programmable (Gascoyne & Vykonkal, 2004); circuits that are oriented to deliver a limited range of frequencies and only sinusoidal waveforms (Manaresi et al., 2003); so-called general purpose systems that are limited in purpose and configurability, varying only in terms of some signal parameters and serving a specific purpose (Tierney, Rader, & Gold., 1971); other systems that do not provide different waveforms nor signal superposition capabilities (Choi et al., 2006); and, finally, systems oriented to one specific application, with no possibilities of being modified (Chang, Lee & Chiu., 2008) (Ibrahim et al., 2009). Applications that use a similar system can be found in many areas, such as nano-manipulation (Villamejane et al, 2010), isolation of malaria (Gascoyne et al, 2002), separation of malignant cells (Alazaam et al, 2008), high voltage stimulation for manipulation (Yuk K. et al, 2007), and micro-fluidics dielectrophoresis (Li, H.