Chapter 4
FPGA Implementations for Chaotic Maps Using Fixed-Point and Floating-Point Representations

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ABSTRACT
This work presents the implementation of various chaotic maps; among the maps there are one-dimensional and two-dimensional ones. In order to implement the maps, their mathematical descriptions are modified to be represented with more accuracy by different binary representations. The sequences from the same map are compared to determine until which iteration, different descriptions produce similar outputs. The similarity coefficient is established in five percent. Comparison delivers some interesting findings; first, the one-dimensional maps, in this work, have comparative number of similar iterations. Second, the bi-dimensional maps present the lowest and highest number of similar iterations. Based on the modified mathematical descriptions, the VHDL implementations are developed. They are simulated and their results are compared against the modified mathematical description ones; resulting that both groups of results are congruent.

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INTRODUCTION

The unusual behavior of chaotic systems has attracted the attention of several scientific communities (Tavazoei & Haeri, 2007). Since chaotic systems are capable of imitating random noise (Persohn & Povinelli, 2012); making them suitable for communications (Sebé & Domingo-Ferrer, 2007), cryptography (Koblitz, Koblitz & Menezes, 2011), computer simulations (Wan & Karniadakis, 2006) and control applications (Wang et al., 2009). Chaos exists in many highly complex nonlinear systems (Yang & Wei, 2008). It possess certain features such as hyper sensitivity to initial conditions, board spectra for its Fourier transform and fractal properties of the motion in the phase plane (Wei-Der Chang, 2008) make them applicable in a wide variety of engineering contexts, for example analog-to-digital converters (Tang, Mees & Chua, 1983), nonlinear oscillators (Deane & Hamill, 1991), random number generators (Espejo, Martin & Huertas, 1990) and signal generators for communications systems (Papadopoulos & Wornell, 1995) and other applications (Rose, 2011). For its practicing, Chaos have been reported even in economics (Puu & Sushko, 2006)

The chaotic system designers always have had a big question about their implementation, his numerical representation (Cristea et al, 2007). If they use fixed-point representation for the system, it will be fast and it could be easily implemented (Sadoudi et al, 2009); however, the system will suffer from a natural degradation (Deng et al., 2015). Many researchers have coexisted with degradation (Shu-Bo et al., 2009); even they have developed certain countermeasures in order to reduce it (Li, Chen & Mou, 2005)(Wang & Yang, 2012). The most common one is to increase the number of bits used for representation (Hu, Deng & Liu, 2014); this remedial minimizes degradation but does not eliminate.

Otherwise, floating-point representation gives a more trustworthy implementation (François, Defour & Negre, 2014); nonetheless, researchers face another problem, this representation requires more complex VHDL codes for its implementation (Sangwan & Yaday, 2010). Additionally, this representation also has limitations because it is digitally implemented; in consequence, degradation stills persist.

The current chapter proposes FPGA implementations for various chaotic maps in different representations. In literature there is certain number of authors that realizes chaos-related FPGA implementation; consequently, we offer a reference-frame of their work with the representation they use and how they implement them (Table 1).

There are some articles that implement chaotic algorithms in a FPGA device; however, no article implements them using floating-point representation by hardware. Moreover, none of the authors makes a comparison about the similarities between fixed and floating point representation; sparking the importance of our proposal as a tool for chaos designers and developers.
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