Chapter 10
Timers and Associated Hardware

INTRODUCTION

This chapter discusses timers 1 through 6. Timers 1, 3 and 5 are 16-bit timers and are very much alike. They are used in conjunction with the CCP (Capture/Compare/PWM) modules. The capture unit is employed to measure pulse durations or clock periods. The compare unit is used to generate periodic signals or pulses. Timers 2, 4 and 6, are 8-bit timers used essentially to generate PWM (Pulse Width Modulation) signals. These signals are important in speed control of motors, dimmers, wireless communications and frequency synthesizers.

TIMER1/3/5

Like Timer0, TimerX is designed to generate periodic interrupts and time delays without burdening the CPU. Figure 1 shows that TimerX is a 16-bit counter that may be clocked internally or externally as specified by TMRxCS<1:0> (TimerX Clock Select bits). When triggered by an external clock, the processor can be operated in the sleep mode. There are two options for the external clock:

- The clock is generated externally via a crystal oscillator or an RC oscillator (e.g., 555 timer chip in astable mode). In this case, the clock signal is fed to the TxCKI pin. Note that T1CKI = RC0, T3CKI = RB5 and T5CKI = RC2.
- The internal oscillator circuit is completed by placing a low frequency crystal (32.768 KHz) between RC0/SOSCO (Secondary Oscillator Output) and RC1/SOSCI (Secondary Oscillator Input). In order to turn on this low power oscillator circuit, TxSOSCEN (Secondary Oscillator Control bit) in TxCON (TimerX Control register) must be set. Besides this, TMRxCS<1:0> (also in TxCON) must be loaded with 10 as illustrated in Table 1.

DOI: 10.4018/978-1-68318-000-5.ch010
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Figure 1. Timer1/3/5 block diagram

Table 1. Clock source selection

<table>
<thead>
<tr>
<th>TMRxCS1</th>
<th>TMRxCS0</th>
<th>TxsOSEN</th>
<th>Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>x</td>
<td>System Clock (Fosc)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>x</td>
<td>Instruction Clock (Fosc / 4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>External Clocking on TxCKI Pin</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Osc. Circuit On SOSCI/SOSCO Pins</td>
</tr>
</tbody>
</table>

Figure 1 also shows the prescaler (frequency divider) with 4 options: divide by 1, 2, 4, and 8. It is controlled by TxCKPS<1:0> in TxCON. The external clock may be fed through a synchronizer \( TxSYNC = 0 \) circuit or may simply bypass this block \( TxSYNC = 1 \). When operating in the sleep mode, the synchronizer must be bypassed. TimerX can be cleared by a special event trigger from the CCP modules.

The figure also shows that TMRxON is used as a clock enable pin. The default value of this flag is logic ‘0’. This means that TimerX is disabled upon reset. When the counter rolls over from 0xFFFF to 0x0000, TMRxIF is set and an interrupt will take place if TMRxIE, GIE and PEIE are all set.

Figure 2 illustrates how TimerX can be read from or written to in one shot. In order to write a 16-bit value to the counter, the user should first write the most significant byte to TMRxH. This value is not latched into TimerX high byte until the user writes to TMRxL. This latching scheme is important in providing the capability of writing a 16-bit value in one shot. By the same token, when TMRxL is read, the upper byte of the counter is transferred to TMRxH and hence a 16-bit count is read in one shot. Table 2 shows the main control register TxCON used to program TimerX. Note that TxRD16 gives the user the option of writing to TimerX in one 16-bit operation or in two 8-bit operations.
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