Chapter 3

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ABSTRACT

In this chapter, the authors explore the estimation of the performances in an earlier stage of (multiprocessors system on chip) MPSoC design in which it is necessary to drive design space exploration and support important design decisions. Therefore, they address the co-design hardware/software with estimating performances in order to find an adequate solution, which consists in mapping the application on the components of architecture with respect the criteria of performance of the system defined from the beginning. The chapter provides a hybrid model for estimating performance in which cohabited simulation and analytical techniques are carried out via a link layer in order to reach an optimal architectural solution quickly. Thus, it allows faster performance estimation with better accuracy at different levels of abstraction.

INTRODUCTION

When one has a set of software and a set of hardware conceived for a specific application, one thus speaks an embedded system. Generally, this last system use microprocessors which necessarily very powerful but are not well adapted for each task. Often, the execution time of a task must be known and limited, and the system must be reliable and secure. The embedded systems are thus very often real time systems. Nowadays, the system micro-electronics is strongly directed towards the mobile and embedded applications such as; PDA (Staff DIGITAL Assistants), GPS (Total Positioning Systems), MPEG4, micro-satellites (Sergio et al., 2011). The multiprocessors systems on chip strongly emerged in this kind of applications (Rousseau et al., 2011), it is for that they become increasingly complex because of their functional constraints (energy consumption (Jayaram et al., 2012), computing power…) and nonfunc-
tional constraints (cost, reliability, Time to Market...) (Smiri et al., 2008) (Hocine et al., 2012) (Philippe et al., 2015). In order to answer the constraints and to find the best trade-offs among performance and cost, the design of system MPSoC should be based on a hybrid approach to performance estimation. Then, one will present initially system MPSoC and in second place, methodologies of MPSoC design by taking examples graphs SDF in analytical model and SoCLib in simulation model. Multi-core Systems-On-Chip MPSoC and Performance Estimation Modeling A multiprocessor system on chip MPSoC is a new generation of architectural System on Chip which makes it possible to raise the challenges of Mono-Processor System on Chip. This system integrates several heterogeneous components such as programmable calculating units and/or nonprogrammable (CPU, DSP, ASICIP, FPGA), components of the complex communication networks (Bus hierarchical on chip, network on chip), the components of memorizing, peripheral I/O, etc. These components integrate on only one silicon part.

Figure 1 illustrates a generic model of a heterogeneous MPSoC system with software and material parts:

- A material node is component which does not have the ability of programming.
- A communication network makes it possible to connect all the nodes together.
- The software nodes make it possible to provide the environment to execute the tasks of the applications.
- The embedded software is structured into layers:
  - Application Layer: This layer represents a set of tasks of the application which are carried out in parallel, in order to profit to the maximum of the parallelism offered by architecture multiprocessors. This layer communicates with the software node by calling on primitives of the operating system (OS).
  - The Operating System OS: The operating system makes it possible to provide an interface between hardware equipment and the application.
  - Libraries: The objective to use the library of communication is to call on the channels of communication and to use the various features of the library C standard and the library of mathematics.
  - Hardware Abstraction Layer: This layer makes it possible the operating system to interact with the material peripherals on a level abstract rather than on a detailed material level.

Figure 1. Typical architecture of a heterogeneous system multiprocessor (Smiri et al., 2008)
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