Chapter 16
Risks Analysis and Mitigation Technique in EDA Sector: VLSI Supply Chain

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ABSTRACT
This chapter describes how as the semiconductor industry is growing at a streaming pace, it comprises a number of global business entities. The industry includes the designing of the VLSI chips, manufacturing of those chips, system integration and the distribution of the VLSI chip. With this the industry has raised the bar among its vendors to provide best possible IC solutions and a highly secure product. The authors thus present this chapter in calculating views on risk involved in this area which are prone to security risks and at the same time focuses on the VLSI supply chain with references to a recent survey that illustrates various ways to handle those risks. In the absence of an effective security mechanism, a varlet here viz. an intellectual property (IP) provider or an integrated circuit design industry, an EDA company, a foundry lab, a distributor of chips or a system integrator, may easily lead to design IP theft or tampering with a designed IC. Since these risks compromise the security system for the VLSI chips, this leads to have a sound security system for an apt risk management.

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INTRODUCTION

In an attempt and designer’s desire to design lightning fast system/network on chips within minimum possible time with best possible constraints, the digital design flow is going towards being fully automated and hence the EDA companies growing in abundance in the market. The need for automation arises because of ample of steps required for a semi/full-custom digital design. Consequently, there also arises possibility of IC theft or IC tamper by an adversary. So there is always a risk involved. To understand those possibilities, we need to generalize some of the most common CAD (Computer aided) design tools that are available in Semiconductor market (Liu B. et al., 2016).

Electronic Design Automation (EDA) Tools

Design Capture Tools

This is the first and most important category of EDA tools since it deals with the designer’s specifications. By capturing here means abstracting and encapsulating a circuit description and preparing the same for further simulations as per SAE (simulation and analysis environment). Collectively, the work at this entry level can be shown by Figure 1.

Simulation Tools

The next set of tools that deal with Front-end IC design. Again these are further classified on the basis of operations performed. One type is for the functional verification of the design, and second one verifying the timing specifications, viz. STA tools, Power analyzers etc. The former one verifies the logic behavior of the IC design corresponding to entry level specification (i.e. in reference to gate level

*Figure 1. Operations performed by Design capture tools*
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