SystemC Language Usage as the Alternative to the HDL and High-level Modeling for NoC Simulation

Aleksandr Romanov, National Research University Higher School of Economics, Moscow, Russia
Alexander Ivannikov, The Institute for Design Problems in Microelectronics of Russian Academy of Sciences, Moscow, Russia

ABSTRACT

This article describes how actual trends of networks-on-chip research and known approaches to their modeling are considered. The characteristics of analytic and high-/low-level simulation are given. The programming language SystemC as an alternative solution to create models of networks-on-chip is proposed, and SystemC models speed increase methodic is observed. The methods of improving SystemC models are formulated. There has been shown how SystemC language can reduce the disadvantages and maximize the advantages of high-level and low-level approaches. To achieve this, the comparison of results for high-level, low-level and SystemC NoC simulation is given on the example of “hot spots” and the geometric shape of regular NoC topologies effect on their productivity.

KEYWORDS
Hot Spots, Hardware Description Language, Network-On-Chip, NOC Modeling, OCNS, NoCtweak, SystemC, System-On-Chip

INTRODUCTION

Continuous development of modern systems on chip (SoC) has led to the emergence of multiprocessor systems. For example, Intel has developed two experimental processors with 48 and 80 cores (Howard et al., 2011); a processor with 167 cores is being developed (Truong et al., 2009); ZMS-40 100-Core StemCell Media processors with Quad ARM Cortex-A9 cores (Huangfu & Zhang, 2015; “ZiiLABS unveils 100-Core ZMS-40 processor”, 2012), TILE-Gx72 with 72 C-programmable 64-bit RISC cores processor and TILE-Mx100 targeting networking with 100 64-bit ARM Cortex-A53 cores processor (“Mellanox Products: TILE-Gx72 Processor”, 2016) is commercially available. Other companies also pursue their ongoing developments.

Multiprocessor SoCs, whose nodes are combined by the total communication subsystem consisting of routers and short connections between them organized as networks, are called networks-on-chip (NoCs). Because they are widespread, the problems of modeling, analysis, and simulation of NoCs are very important.

The article consists of the following sections: statement of the problem and objectives of research; analytical, low-level and high-level NoC modeling characterization; SystemC as a compromise between high level and low-level modeling; description of method of HDL-model translation into SystemC language; comparison of SystemC and high level OCNS NoC models, and comparative analysis of the simulation time for the different models of the different levels.
STATEMENT OF THE PROBLEM AND OBJECTIVES OF RESEARCH

According to Marculescu et al. (2009), basic directions of current research on the subject of NoCs are:

1. Modeling of network traffic and creating the appropriate test tasks.
2. Display of the problems on NoCs and their planning.
3. Routing and flow control in the NoCs.
4. Ensuring the required quality of service.
5. Management of power, temperature control and timing.
6. Reliability and fault tolerance of the NoCs.
7. Creation of the optimal topology of NoC connections.
8. Development of an effective structure of routers and network channels.
9. Scheduling of NoC deployment.
10. NoC prototyping, testing, and verification.
11. NoC modeling, analysis and simulation.

A large number of research areas reflect the complexity of NoCs as an object of research. It should be also emphasized that on NoC modeling, analysis, and simulation, other areas of search are based. Therefore, the choice of adequate methods and tools for NoC modeling is challenging.

Analytical NOC Modeling

NoC modeling aims to obtain and analyze critical network characteristics such as bandwidth, energy and resource consumption, resistance to bugs and others. Depending on the purpose of the study, the models can be of different level of abstraction and therefore have a different accuracy and the time required for modeling.

A typical approach involves an output, analysis and analytical approximation of formula dependencies that describe the processes occurring in NoCs or their characteristics.

In general, the process of NoC synthesis can be implemented by mapping an application problem characteristic graph (APCG) onto NoC architecture. APCG is \( G = (C, A) \), a directed graph, where \( C \) – set of vertices that characterize computing nodes, \( A \) – set of communication processes between nodes. In turn, NoC architecture is characterized by: \( T(R, Ch) \) topology, where \( R \) and \( Ch \) – sets of routers and physical links between them; a routing mechanism (\( P \)); a function of mapping of APCG vertices onto NoC routers (\( \Omega (C) \)).

According to the above definitions, it is possible to bring out communication energy cost dependence:

\[
E = \sum_{a_{i,j}} v(a_{i,j}) \times E_{bit}(\Omega(c_i), \Omega(c_j))
\]

where \( v(a_{i,j}) \) – capacity of communication process between nodes \( i, j \); \( E_{bit}(\Omega(c_i), \Omega(c_j)) \) – energy spent on 1 bit of data transfer between nodes \( c_i \) and \( c_j \).

Communication energy minimization problem has to be solved by finding such \( \Omega (C) \), that arranges for connections of communication process with high capacity to have a low energy consumption for transferring 1 bit. For some regular NoC topologies, this problem is partially solved by Hu and Marculescu (2003), but not for irregular topologies, so modeling of NoCs to find optimal solutions remains an important task. Equation (1) is fundamental, and all researches to find optimal NoC topologies for a particular problem, in one form or another, can be referred to an attempt to minimize this function.
Optimized Communication Architecture of MPSoCs with a Hardware Scheduler: A System-Level Analysis
www.igi-global.com/chapter/optimized-communication-architecture-mpsocshardware/74247?camid=4v1a

String-Based Feature Representation for Trajectory Clustering
www.igi-global.com/article/string-based-feature-representation-for-trajectory-clustering/225485?camid=4v1a