Chapter 17

Optimization of Dynamic Power for System on Programmable Chip SOPC: Power Optimization

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ABSTRACT

In this chapter, the authors present a new scheduling algorithm that brings a reduction in dynamic power consumption by achieving components scheduling while holding the global latency of the application. The main idea of that algorithm is to augment the latency of some components without impacting the dependency constraint and degrading the global latency of the system. There exist many solutions that manage to increase component’s latency; one of them is through decreasing the frequency of their corresponding clocks. Generally, such a method leads to an augmentation in global latency of a system. However, this algorithm manages to reduce the consumed power and hold the same global latency of the system. The presented algorithm has been tested and it provides a significant gain in power at both simulation and physical levels.

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INTRODUCTION

Currently, the implementation of electronic systems leads to two main directions. The first one is summed up by the increasing complexity and the second one is reflected in significant functional variability. According to the famous law of Moore, a migration towards geometries of technological smaller processes is noticed. Therefore, it is expected today to have more than 12 billion transistors per chip when using a standard 20 nm technology. The number of transistors reached a level of 7.1 billion and 2.6 billion in Graphics Processing Units (GPUs) and general purpose microprocessors, respectively. The second direction, attempts to integrate various complex functions with higher performance. Applications Specific Integrated Circuits (ASICs) with a number of transistors greater than 200 million per chip and standard parts (ASSP) applications with transistors greater than 100 million per chip will be replaced by System in Package (SiP) and System on Chip (SoC). Practically speaking, 70% to 80% of today’s integrated circuits are System on Chips, ranging from targeted applications to new microprocessors and integrated telecommunications systems.

The quality / performance of these devices is not only measured by what types of features these devices are capable of, but also how long these gadgets survive without being plugged into the supply voltage to be recharged. There is an increased demand for a reduced form factor or a smaller size of such devices, which is generally determined by the power consumption of such devices.

Since power dissipation is one of the most important parameters that improve the reliability and performance of these systems, power minimization has become a vital and critical aspect while creating a system on chip. Although embedded systems seem to be able to meet the demand for processing power and flexibility of complex applications, such systems are very complicated to design and optimize. Thus, the design methodology plays a major role to ensure the product success.

Without a well-established methodology for design and verification, the complexity of these circuits results in an increasing number of functional errors, which can lead to failures and multiple re-designs. Previously, the conventional design of a heterogeneous embedded system consists on carrying out the algorithm design, the hardware design and the software design separately and sequentially. Given that the expected growth rate of conventional design productivity is much lower than the complexity of the system, a new approach has emerged as a new design methodology in recent years. It is called hardware / software (HW / SW) co-design.

This methodology is divided into two levels: high level and low level. Traditionally, the hardware design flow begins with the register transfer level (RTL) arriving to the logic level and ending with the realization of the circuit. The methods of power estimation and optimization at the low level have been widely studied. However, the increase in current demand and the reduction of time-to-market of electronic equipment has forced designers to adopt high-level models in their design flow. Thus, high-level techniques have become the vital today’s requirement.

Several techniques have been proposed in order to have a less consumable and more reliable systems. These techniques are situated on several levels of abstraction while impacting with a different way the final consumption of the circuit.

High level synthesis is a process of translating a behavioral description into a set of connected storage and functional units. The basic operations executed in high-level synthesis are partitioning, scheduling and allocation. The partitioning algorithms divide a behavioral or structural description into subscriptions in order to reduce the size of the problem or to satisfy certain external constraints. Scheduling
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