Chapter 11

Ultra-Low-Power Strategy for Reliable IoE Nanoscale Integrated Circuits

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ABSTRACT

Ultra-low-power strategies have a huge importance in today’s integrated circuits designed for internet of everything (IoE) applications, as all portable devices quest for the never-ending battery life. Dynamic voltage and frequency scaling techniques can be rewarding, and the drastic power savings obtained in subthreshold voltage operation makes this an important technique to be used in battery-operated devices. However, unpredictability in nanoscale chips is high, and working at reduced supply voltages makes circuits more vulnerable to operational-induced delay-faults and transient-faults. The goal is to implement an adaptive voltage scaling (AVS) strategy, which can work at subthreshold voltages to considerably reduce power consumption. The proposed strategy uses aging-aware local and global performance sensors to enhance reliability and fault-tolerance and allows circuits to be dynamically optimized during their lifetime while prevents error occurrence. Spice simulations in 65nm CMOS technology demonstrate the results.

INTRODUCTION

In today’s Integrated Circuits (IC) two important requirements are size and power consumption, which optimally should be the lowest possible. Particularly in IC and cyber-physical systems developed for Internet-of-Everything (IoE) applications, size and power impose the use of state-of-the-art CMOS nanotechnologies. Moreover, the IoE paradigm is enabling the interaction with a wide variety of devices, which tend to be self-powered and equipped with complex digital systems, including microcontrollers, sensors and sensor networks. Therefore, power consumption in CMOS integrated circuits, as never before, has a huge importance in today’s chips for IoE applications, as all self-powered devices quest for the never-ending battery life, but also with smaller and smaller dimensions every day, in order to be used widely. However, the use of reduced CMOS technology with reduced power budgets imposes additional reliability challenges for such hardware, which must be considered earlier since the design stage, to guarantee that circuits will operate with no errors. Therefore, reliability and power consumption are two key concerns in the development of today’s IoE chips.

Several low-power techniques are available to reduce consumption in today’s chips. In energy savings techniques, the bottom line is to use power only when needed. In this way, aggressive techniques like power-gating are gaining ways in several application levels of abstraction. Not only at transistor level, where the classical power-gating is used, but also at system-level, where programmable RTC (Real-Time-Clocks) are being widely used to power-off the circuit to the minimum operation, in order to reduce power consumption when it is not needed. Then, periodically and sparsely in time, the RTC will wake-up the system and allow the minimum operation time to perform the required operation, so it can put the system back to sleep again.

In addition, Adaptive Voltage and Frequency Scaling (AVS) techniques and Dynamic Voltage and Frequency Scaling (DVFS) techniques can be very important to reduce performance and power consumption when it is not needed. The future requirements of IoE devices tend strongly towards the reduction of power consumption even at the expense of some performance reduction, as the energy efficiency paradigm becomes increasingly important. IoE applications require the use of nearly-zero power consumption sensors, to be available while gathering data from everywhere using nearly-zero energy, and sparsely can transmit these data to the web. These never-ending battery achievements can only be achieved with more than one technique, and working at different power supply voltage (VDD) and clock frequency levels.

However, in order to further increase energy savings, the DVFS techniques can be taken to the limit, by reducing the supply voltage to subthreshold voltage levels in the power-supply. In this case, clock frequency must also be drastically reduced, to guarantee a fail-safe operation. Subthreshold operation has already been studied in the past, and the work of Calhoun, Benton H. et al. (2005), Keller, Sean et al. (2011) Radfar, Mohsen et al. (2012), Hanson, S. et al. (2008), Giustolisi, G. et al. (2003), Kim, Jae-Joon et al. (2004), Li, Ming-Zhong et al. (2013), and Sahu, Alok et al. (2014), are several examples of previous works dealing with subthreshold voltage operation. However, working at subthreshold voltage levels puts digital CMOS circuits in a very vulnerable and unreliable situation. The reduced energy available in the circuit considerably reduces performance and considerably increases variability. Errors are more prone to happen, especially due to: transient faults, operation induced delay-faults, process variations, power-supply variations, temperature variations, electromagnetic interference (EMI), single-event upsets (SEU), radiation, etc… Fortunately, aging degradations caused by effects such as Bias Temperature Instability (BTI) are reduced, due to the reduced voltages applied to transistors’ gates.