Cooperative Encoding Strategy for Gate Array Placement

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ABSTRACT

In recent years, the quadratic force-directed placement is becoming popular due to its stable quality at low power. The force-directed placement composes of two operations, namely, orientating and modulating. The two actions are going on until the overlap degree can meet a predetermined target. Different methods have a great influence on their quality of a layout. A novel encoding strategy of two-dimensional chromosome based on immune cooperative optimization is suggested. The main works first focus on a multi-point crossover strategy, and its Poisson distribution makes use of a Euclidean distance density between the concentration of antibody suppression and the translation variation of optimal gene pairs in two-dimension. Then, a flexible region division is proposed for dealing with the layout problem of gate array. The related experiment indicates the constructed encoding strategy for gate array placement is effective and efficient.

KEYWORDS

Cognitive Informatics, Density Euclidean Distance, Gate Array Placement, Immune Optimization

INTRODUCTION

The requirement of the scale and function of the integrated circuit has been continually raised, which relies more on automation and auxiliary design (Andrew et al., 2011; Chen, 2012). According to the rules of the circuit structure and classification, the layout process divides into three different modes: gate array, standard unit and macro module (variable shape or soft) (Zhao, 2006). Among them, the gate array mode has advantages of short design cycles and low cost for its design and so on, and it can be accomplished fast and effectively by using automatic routing technology (Chu, 2008).

In the past thirty years, the placement and routing algorithms have been widely concerned and studied by the related researchers. Some intelligent placement algorithms basing on random optimization have been proposed, for example, using Tabu search (Ren, 2011), simulated annealing, particle swarm optimization, and other algorithms to solve the placement problem, detailed in (Xu, 2002; Pan, Viswanathan & Chu, 2005).

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Despite many years of research and practice on integrated circuit layout, many problems of IC design are becoming more and more complex, and the ability to use traditional methods to solve problems is becoming more and more limited. For example, the evolutionary operator in genetic algorithm provides opportunities for every individually and then makes the whole population have the possibility of degenerating inevitably. And then it is likely trapped in local optimum. Consequently, the global optimum of the model could not be found accurately and quickly.

The immune optimization is inspired by the biological immune system, which can use prior knowledge or characteristic information of most problems to be solved in order to mitigate the degeneration in the process of evolution. Through recognition of different antigen types of gene, the antibody to different types of genes can be produced. Through mechanisms of auto-regulation to promote the emergence of new individual genes and restrain too much generation of individuals having similar genes, thereby, maintaining the diversity of the antibody population (Yan, 2008). Immune algorithm maintains the diversity of the antibody population, which has a positive effect on the problem of the integrated circuit layout trapping in local optimum (Wang et al., 2012). Because of these discussions, this article applies the improved immune optimization into the gate array layout.

**PROBLEM DESCRIPTIONS**

The core of IC gate array layout problem focuses on the optimal combination of gate array units, which means to place n units according to some patterns of gate array in order to meet different constraints of integrated demand (Tim, 2011; Stephen, 1992).

**Some Definitions**

The information determined in the stage of circuit design before gate array layout includes the following: (1) The unit number of gate array n, the height of each gate array unit \( h_i \) and the width of each gate array unit; (2) Coordinates of gate array unit I/O pins; (3) A set of gate array line network \( L \). Coordinates of each I/O pins where every line network linked to. (4) The height \( H \) and width \( W \) of gate array layout zone. Number of lines \( r \) which layout zone been divided into and the height of each line \( h_i() \).

Each gate array line network \( L \) can be linked to two or more gate array units \( A_j \) or pins \( P_i \), a gate array unit \( A_j \) or pin \( P_i \) belongs to multiple gate array line networks.

**An Example of Layout**

Figure 1 takes a 6×6 gate array as an example of the immune optimization algorithm according to the modified structure for the classical requirement.

![Figure 1. Benchmark circuits’ classical layout](image-url)
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