Chapter 2

Low-Power High-Performance Tunnel FET With Analysis for IoT Applications

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ABSTRACT
The emerging tunnel FET is analysed in terms of ON-state current, OFF-state current, subthreshold slope, switching capacitance to explore its applications for smaller size low-power high-speed digital and memory applications that are an integral part of portable intelligent devices for IoT applications. A large portion of IoT systems are associated with these embedded SRAM/DRAM memories that contribute to a major portion of power dissipation in systems-on-chip (SoCs) or digital design. Several SRAM cell-based memory designs with TFET structures are compared to focus their applications. The ambipolar nature of TFET structures are investigated for highly random, unclonable secured hardware systems. New circuit designs with TFET were explored for turn-on voltage reduction, ON-state resistance reduction, and reverse leakage reduction techniques that plays an important role in designing efficient energy-harvesting systems.

TRANSISTOR DESIGN FOR IOT SYSTEMS
The significant growth in the amount of data to be processed, transmitted, and stored by IOT systems focuses the concern toward low power secured hardware structures. A low energy secured system requires new researches at different level of micro-architectures, gate level/register transfer level and transistor level design (Taheri et al, 2017). The increasing demand of Internet of Things (IoTs) as a future perspective of electronics industry requires highly energy efficient design of sensor nodes. Several IOT based applications such as sensing hazardous environmental conditions, wearable and portable health monitoring system, bio-medical sensors, remote surveillance, traffic monitoring and other sensing network require ultra-low high speed, low power and energy-efficient devices to maintain long battery life as well as embedded self energy harvesting technique (Ahmad et al, 2018). A large portion of IOT systems

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are associated with these embedded SRAM/DRAM memories that contribute to major portion of power dissipation in Systems-on-Chip (SoCs) or digital design (Lee et al, 2013). The flip-flops are critical components in any SoC design, so Some of literature shows flip-flop designs with FETs especially for microprocessor based systems and digital logic where flip-flops are used as pipeline registers, register files and buffers (Rasouli et al, 2006; Gupta et al, 2016). These flip-flop supports voltage scaling and works for supply voltages from 0.3V to 0.6V with improved leakage by 4 to 7 decades with advance transistor designs. The designer task is achieving secured low power micro-architectures by taking consideration for functionality, performance, power, area and overall cost. The new transistors are coming into picture with advance features to replace CMOS technology removing the scaling barriers. The technology must have some distinguished feature and performance that can be implemented for secured IOT systems with low energy. The transistors based on new technology must design by taking care for, fault models, manufacturing defects and reliability issues.

ADVANCE TUNNEL FET STRUCTURES

Increasing need for smart devices based on internet-of-thing (IOT), focuses the designer concern for new emerging solid state transistors other conventional MOSFET. This work deals with the analysis of Tunnel FET to optimise device performance for low power, high switching speed circuit enabling its use in smart applications. Low voltage application of Tunnel FET with steep subthreshold slope, has potential to replace its MOSFET counterpart for future scaling due to thermal limits imposed on nano-level transistors. Longer channel region increases the tunneling area results in increasing tunneling current and decreasing miller capacitance to improve device switching performance for digital application. The Tunnel FET has significant potential to overcome limitations imposed due the scaling in low voltage region because of its steep subthreshold slope that leads to abrupt transition from ON-state to OFF-state. Use of Si$_0.7$Ge$_{0.3}$ material as pocket region (0.5nm) enhances band-to-band tunneling by decreasing tunneling distance. The Si$_{0.7}$Ge$_{0.3}$ pocket region also provide additional barrier to OFF-state leakage leading to the reduction in leakage current drastically resulting in to low static power consumption. Si-SiGe interface is utilised because of its better matching and easier fabrication steps as compared to other available hetero-junction structures. The proposed pocket ultra-small pocket Si$_{0.7}$Ge$_{0.3}$ Junction-less TFET (JLTFET) exploits advantage junction-less regions and p-type pocket region to improve device performance in subthreshold region showing improvement in subthreshold slope and better ON and OFF-state drain current ratio as compared to other similar TFET structures. Proposed ultra-small pocket JLTFT shows high value $I_{on}/I_{off}$ ratio and good subthreshold behaviour even with 2nm gate length and body thickness 0.5nm that can be part of efficient digital and memory applications with lesser occupancy of silicon area compatible to portable and wearable smart devices. All the analysis and verification for proposed JLTFT carried out on Visual TCAD 2D/3D device simulator.

Technology scaling imposes conditions on subthreshold performance of transistors. The subthreshold slope (SS) limitation of 60mV/decade is the major challenge for CMOS at room temperature and, that imposes restrictions on further reduction of static power consumption in CMOS based memory designs. The MOSFET switching process based on the temperature-dependent model of electrons injection over the barrier that restricts the transition slope steepness to be scaled further in terms of ON/OFF currents (Taur et al, 2013). A novel inter-band tunnel FET was introduced to provide steeper sub-threshold slope (<60 mV/decade) (Fan et al, 2016) and low static power consumptions. Hetero-junction vertical p and
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