Chapter 10
Design for Testability of High-Speed Advance Multipliers: Design for Testability

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ABSTRACT
An efficient design for testability (DFT) has been a major thrust of area for today’s VLSI engineers. A poorly designed DFT would result in losses for manufacturers with a considerable rework for the designers. BIST (built-in self-test), one of the promising DFT techniques, is rapidly modifying with the advances in technology as the device shrinks. The increasing complexities of the hardware have shifted the trend to include BISTs in high performance circuitry for offline as well as online testing. Work done here involves testing a circuit under test (CUT) with built in response analyser and vector generator with a monitor to control all the activities.

INTRODUCTION
This chapter covers a basic introduction to testing, problems incorporated, Built-in-Self Test (BIST) (Stroud, 2002 & Hussain, 2013) including the major advantages and disadvantages of BIST along with its hardware implementation. The aim here is to launch the basic ethics of BIST and how it fits into the overall testing process. Therefore, a general description of testing is illustrated to explain the imperative aspects of testing that are needed for implementation of BIST module on FPGA kit. Secondly, a fault model is proposed for the 4-bit Wallace tree multiplier circuit and test pattern generated. The verification of different fault models has been carried out using FPGA board for reliable operation of the multiplier. In high performance systems such as a microprocessor, DSP, etc. the arithmetic addition and multiplication of two binary numbers are fundamental and most often used operations. This work presents the process of design implementation for a complete BIST working on both normal operation mode as well as test mode for a 4 -bits Wallace tree multiplier circuitry.

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MULTIPLIER

Multipliers are now becoming an integral part of today’s digital circuit such as a microprocessor, DSP, etc. The addition and multiplication are fundamental arithmetic operations for two binary numbers. It was found that 70% DSP and microprocessor instructions are based on addition and multiplication operations and dominates the overall execution time. So, the high-speed processing has become a demand with expanding computer and signal processing applications. The DSP based multiplier must be designed for low power dissipation. An optimized number of operation leads to a reduction in dynamic power consumption and hence reducing total power consumption. So, the designer must concentrate on low power-efficient and high-speed circuit design. The objective should be designing a physically packed multiplier with high speed and low power dissipation. A two operand addition circuit with radix-4 partial-product generation and an addition were used to implement 2’s-complement array multipliers. A modern Xilinx FPGAs was used that is based on a 6-input LUT architecture for the implementation of high performance array multiplier (Walter, 2016). A fast Montgomery multiplier was proposed using Vertex-7 FPGA that works iteratively where a digit of an operand is multiplied by another digit of an operand, the accumulated result is reduced by Montgomery method (Erdem, 2018). Here, in the present chapter, a 4-bit Wallace tree multiplier is designed on FPGA Artix-7 board for the delay, power and fault analysis. The fault analysis is described with stuck-at and bridging fault models for 4-bit Wallace tree multiplier.

WALLACE TREE

A Wallace tree multiplier is an efficient digital hardware implementation that multiplies two numbers devised by scientist Chris Wallace. The Wallace tree uses carry select adders for the addition of optimum generated partial products. The Wallace tree has three steps:

- Each bit of the arguments is multiplied by each bit of the other, resulting $n^2$ results. Resulting wires carry different weights depending on the position of the multiplied bits.
- Reduced the number of partials products to two by layers of full and half adders.
- Two-wire groups are there that are added with a conventional adder.

FIELD PROGRAMMABLE GATE ARRAY (FPGA)

The Nexys4 board is an user-friendly digital circuit development board based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx. The large and high- capacity FPGA (Xilinx part number XC7A100T-1CG324C) has generous external memories, Ethernet, collection of USB and other ports. Designers can implement introductory combinational circuits to powerful embedded processors on Nexys4 board (Figure 2). Nexys4 board has several built-in peripherals such as accelerometer, MEMs digital microphone, temperature sensor, speaker amplifier and I/O devices that allow a wide range of designs implementation without needing any other components.

The Artix-7 FPGA offers more capacity, higher performance, and more resources than earlier designs. Artix-7 100T description include:
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