Chapter IX

Design and Implementation of Multirate Digital Filters

Håkan Johansson and Lars Wanhammar
Linköping University, Sweden

In this chapter we discuss techniques to design and implement multirate digital filters with low power consumption which also allow a reduction in the design effort, since the resulting circuits are highly modular and regular and can relatively easily be incorporated in the normal design flow of commercial tools. First we briefly review techniques that can be applied at various design levels, i.e., from algorithm level down to layout, to reduce the power consumption in CMOS implementations of both digital FIR and IIR filters and are useful in many other DSP algorithms. Second, we discuss the properties of lattice wave digital filters and various techniques to design efficient multirate digital filters for changing the sampling rate by a factor of two. Third, we discuss the design of multistage multirate digital FIR filter structures for arbitrary bandwidths. Finally, we provide some design examples.

IMPLEMENTATION ASPECTS

Until recently throughput and chip area were the main metrics for evaluation of DSP algorithms and their implementations. However, with the advancement of CMOS technology it is no longer a major problem to achieve high enough throughput and the cost of the chip area can usually be neglected, except in very high-volume products. Today, the focus should instead be placed on design efficiency and low power consumption, since many implementations are battery-powered and too high power dissipation may require more expensive packaging and cooling. Further, there is also a strong trend to

use more a sophisticated and complex digital signal processing which tends to increase the power dissipation.

In this chapter we discuss techniques to design and implement multirate digital filters with low power consumption that also allow a reduction in the design effort, since the resulting circuits are highly modular and regular and can relatively easily be incorporated in the normal design flow of commercial tools.

**Power Consumption in CMOS Circuits**

CMOS technology is currently and will continue to be the dominating technology for VLSI and ULSI circuits. The feature size is rapidly shrinking towards 0.1-µm and below. Circuits implemented using modern CMOS processes are no longer characterized by the number of transistors on the chip. Instead, the overall throughput and power consumption are more appropriate metrics.

Here we assume the digital filter is operated continuously and therefore the leakage and short-circuit currents can be neglected (Chandrakasan, 1995). The power dissipation associated with switching in CMOS circuits is approximately given by

\[ P = \alpha f_{CL} C_L V_{DD} \Delta V_{DD} \rightarrow \alpha f_{CL} C_L V_{DD}^2, \]

where \( \alpha \) is the activity factor, i.e., the average number of transitions for the equivalent electrical node per clock cycle, \( f_{CL} \) is the clock frequency, \( C_L \) is the equivalent switched capacitance of the whole circuit, \( V_{DD} \) is the power supply voltage, and \( V_{DD} \) is the voltage swing. In most cases we use CMOS circuits with full swing, i.e., \( V_{DD} = V_{DD} \).

Using a special low-power CMOS process can, of course, reduce the power consumption of digital circuits. Here, however, we will assume that the digital filters will be implemented using a standard digital CMOS process. Reducing any of the factors in Equation (1) can decrease the power consumption. Below we briefly review various techniques that can be applied to reduce the power consumption in digital filters and are useful in many other DSP algorithms.

**Activity Factor**

The activity factor \( \alpha \) can be reduced in several ways. Most techniques exploit known statistical properties of the signals. For example, operations to be executed on an adder or multiplier can be scheduled with respect to the correlation between successive operands so that the carry propagation and glitches are minimized. For example, in the first moment only the first full-adder (LSB) in a bit-parallel ripple-carry adder has correct inputs and performs a
Related Content

Symbolic Model Checking for Interlocking Systems
[www.igi-global.com/chapter/symbolic-model-checking-interlocking-systems/66677?camid=4v1a](www.igi-global.com/chapter/symbolic-model-checking-interlocking-systems/66677?camid=4v1a)

Methodologies for Active Knowledge Modeling
[www.igi-global.com/chapter/methodologies-active-knowledge-modeling/23786?camid=4v1a](www.igi-global.com/chapter/methodologies-active-knowledge-modeling/23786?camid=4v1a)

To Prevent Reverse-Enginnering Tools by Shuffling the Stack Status with Hook Mechanism
A Platform for Analyzing Behaviors of Service-Oriented Application Based on the Probabilistic Model Checking
International Journal of Software Innovation (pp. 24-38).
www.igi-global.com/article/a-platform-for-analyzing-behaviors-of-service-oriented-application-based-on-the-probabilistic-model-checking/122791?camid=4v1a