Chapter 9

SystemC Platform Modeling for Behavioral Simulation and Performance Estimation of Embedded Systems

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ABSTRACT

Currently, embedded systems make use of large, multiprocessing systems on chip integrating complex application software running on the different processors in close interaction with the application-specific hardware. These systems demand new modeling, simulation, and performance estimation tools and methodologies for system architecture evaluation and design exploration. Recently approved as IEEE 1666 standard, SystemC has proven to be a powerful language for system modeling and simulation. In this chapter, SCoPE, a SystemC framework for platform modeling, SW source-code behavioral simulation and performance estimation of embedded systems is presented. Using SCoPE, the application SW running on the different processors of the platform can be simulated efficiently in close interaction with the rest of the platform components. In this way, fast and sufficiently accurate performance metrics are obtained for design-space exploration.

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INTRODUCTION

Current integrated circuit technologies allow the implementation of general-purpose processors and application-specific HW in a single chip leading to what is called, Systems on Chip (SoC). The tendency continues towards SoC containing multiple processors executing SW in parallel. In this way, the SoC become Multi-Processing SoC (MPSoC) (Jerraya & Wolf, 2005). Moreover, the interactions among so many computational units make traditional bus-based architectures unscalable and unfeasible for efficient MPSoC communication. The increase of collisions and delays produced in buses obliges a move to Network on Chip (NoC) architectures (Benini & de Micheli, 2006).

Design productivity for these complex, integrated systems remains one of the Grand Challenges to the evolution of the semiconductor technology, as stated by the ITRS (ITRS, 2007A). In fact, “cost of design is the greatest threat to continuation of the semiconductor roadmap”. An essential aspect to be highlighted is that “SW aspects of Integrated Circuit (IC) design can now account for 80% or more of embedded system development costs” (ITRS, 2007B, p. 1).

Correct dimensioning of the system at the beginning of the development process is a key design decision to ensure an optimized implementation. System design with an optimum trade-off in performance and cost requires the consideration of a wide set of parameters, such as number and type of processors, mapping of SW tasks and suitability of communication infrastructure. This wide set of system parameters implies a wide design space to be explored by the system designer.

Design Space Exploration (DSE) enables the designer to evaluate different possibilities in order to implement the design covering the requirements in an efficient way. Once the system specification has been developed, and before fine grain refinement, all the relevant possibilities have to be explored. This exploration of the design space consists in analyzing the characteristics of the possible system configurations in terms of performance, power, area, cost, etc.

Due to the large number of possibilities to be analyzed, fast and sufficiently accurate modeling and simulation techniques are required. As a consequence, fast simulation and performance analysis is necessary with enough accuracy in the metrics provided in order to enable an adequate system evaluation. Estimation errors of about 30-40% can be accepted for initial system assessments (ITRS, 2007).

System modeling, simulation, performance analysis and design-space exploration are fundamental Electronic, System-Level (ESL) design activities. ESL design is currently a very active area including any electronic design methodology that focuses on higher abstraction levels than RTL (Bailey, Martin, & Piziali, 2007). The basic premise is to model the behavior of the entire system using languages that support higher abstraction levels than VHDL or Verilog. Among them, C, C++, MatLab-Simulink, SystemVerilog and SystemC are the most popular ones. ESL is now an established market and most of the world’s leading SoC CAD companies offer different tools tackling different design steps.

Currently, two different approaches to system modeling and simulation can be found (Milligan, 2005). On the one hand, high-level, behavioral models such as C/C++ or MatLab-Simulink are used. They are fast but do not provide information about the performance of a particular architectural solution. On the other hand, there are cycle-accurate models based on ISS simulation of the complete application SW and Real Time Operative System (RTOS) on each processor interacting with the application-specific HW using a Transaction Level Modeling (TLM) interface. They are precise but too slow for performance analysis and architectural exploration.

In this chapter, SCoPE, a SystemC framework supporting platform modeling for behavioral simulation and performance estimation of embedded systems is proposed. The execution of the applica-