Parallelization and Performance Evaluation of an Edge Detection Algorithm on a Streaming Multi-Core Engine

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ABSTRACT

In the world of multi-core processors, the STI Cell Broadband Engine (BE) stands out as a heterogeneous 9-core processor with a PowerPC host processor (PPE) and 8 synergic processor engines (SPEs). The Cell BE architecture is designed to improve upon conventional processors in graphics and related areas by integrating 8 computation engines each with multiple execution units and large register sets to achieve a high performance per area return. In this paper, we discuss the parallelization, implementation and performance evaluation of an edge detection image processing application based on the Roberts edge detector on the Cell BE. The authors report the edge detection performance measured on a computer with one Cell processor and with varying numbers of synergic processor engines enabled. These results are compared to the results obtained on the Cell’s single PPE with all 8 SPEs disabled. The results indicate that edge detection performs 10 times faster on the Cell BE than on modern RISC processors.

Keywords: Cell Broadband Engine, Edge Detection, Multi-Core Computing, Roberts Edge Detector

INTRODUCTION

The Cell Broadband Engine (BE) is a 3.2GHz heterogeneous multi-core microprocessor designed by STI (Sony, Toshiba, IBM) to achieve high performance computation for graphics, imaging and visualization applications, and generally to a wide scope of data parallel applications. It is composed of one 64-bit PowerPC Processing Element (PPE) serving as host processor, eight specialized co-processors called Synergistic Processing Elements (SPE) each with multiple integer and floating point execution units with vectorization capability, and one internal high speed bus called Element Interconnect Bus (EIB) which links PPE and SPEs together (IBM Corp.). The host PPE supports the 64-bit PowerPCAS instruction set architecture,
and the VMX (Altivec) vector instruction set architecture to parallelize arithmetic operations. Each SPE consists of a Synergistic Processing Unit (SPU), and a SMF unit providing DMA (direct memory Access), memory management, and bus operations. A SPE is a RISC processor with an in-oder dual-issue medium-size pipeline and a 128-bit SIMD organization for single and double precision instructions. Each SPE contains a 256KB instruction and data local memory area, known as the local store or LS for short, which is visible to the PPE and can be addressed directly by software. The local store does not operate like a superscalar CPU cache since it is neither transparent to software nor does it contain hardware structures that predict what data to load.

The EIB is a high bandwidth circular bus made of two channels in opposite directions (precisely, 1 address bus and 4 16B rings, each pair of rings runs in opposite directions) and allows for communication between the PPE, SPEs, memory and I/O. The Cell BE can handle 10 simultaneous threads and over 128 outstanding memory requests.

The following sections describe the edge detection application which we parallelized and developed on the Cell BE (Kidwai, Sibai, & Rabie, 2008), and the programming model chosen for it. Implementations on both PPE only (serial) and PPE-SPE (parallel or embedded) with varying number of SPEs are described. This is followed by the presentation of the execution times in each implementation and speedup analysis.

**EDGE DETECTION**

Detecting edges is a fundamental application in image processing and early computer vision. The edges of objects appearing in an image hold much of the information in the image. The image edges give the locations of where items are, their size, shape, and something about their texture. An edge is where the gray level of the image moves from an area of low values to high values or vice versa (Canny, 1986; Der-
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