Chapter 14
Enhancing the Efficiency of Memory Management in a Super-Paging Environment by AMSQM

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ABSTRACT

The concept of Super-Paging has been wandering around for more than a decade. Super-Pages are supported by some operating systems. In addition, there are some interesting research papers that show interesting ideas how to intelligently integrate Super-Pages into modern operating systems; however, the page replacement algorithms used by the contemporary operating system even now use the old Clock algorithm which does not prioritize small or large pages based on their size. In this chapter an algorithm for page replacement in a Super-Page environment is presented. The new technique for page replacement decisions is based on the page size and other parameters; hence is appropriate for a Super-Paging environment.

INTRODUCTION

The paging concept is very old and well-known. Super-Paging is an augmentation for this well-known concept. Super-Pages are larger pages that are pointed to by the TLB (Khalidi et al., 1993). The internal memory of modern computers has been drastically increased during the last decades. However, the TLB coverage (i.e. the size of the memory that can be pointed to directly by the TLB) has been increased by a much lower factor during the same period (Navarro, 2004), (Navarro et al., 2002). Therefore, several new architectures like Itanium, MIPS R4x00, Alpha, SPARC and HP PA RISC support multiple page size of the frames pointed to by the TLB. In that way the memory size pointed to directly by the TLB is higher and the overhead of the page table access time is reduced. There are also some particular operating systems
that support Super-Paging e.g. (Ganapathy and Schimmel, 1998), (Subramanian et al., 1998), (Winwood et al., 2002).

The Super-Paging concept brings up several questions to discuss in the operating systems community. First, when should the Operating System upgrade some base pages into a large Super-Page? This dilemma is even more complicated when the processor supports several sizes of Super-Pages; e.g. the Itanium has 10 sizes of Super-Pages. Second, where should the location of the small pages in the memory be? One possibility is placing them in a location that spares the need for relocation of the base page, once the Operating System upgrades base pages into a Super-Page (Talluri and Hill, 1994). Another policy is placing the base page in the first vacant location in the memory and relocating it when the Operating System upgrades (Romer et al., 1995). Thirdly, who handles the relocation, the hardware or the software (Fang et al., 2001)? Some processors and Operating Systems have addressed these questions as was mentioned above. More about Super-pages can be read at (Wiseman, 2005).

In this chapter a new algorithm for page replacement in a Super-Paging environment is suggested (Itshak and Wiseman, 2009). The new algorithm is based on some parameters including the page size. The results show better TLB miss rate for the benchmarks used for testing.

Multimedia applications typically have large portions of memory that are clustered in few areas. Such applications can benefit Super-Paging enormously (Abouaissa et al., 1999). Also, nowadays computers usually have large memories (Wallace et al., 2006), (Geppert, 2003); hence, larger pages can be used; however using larger pages can apparently cause a higher page fault rate. This is a well-known flaw of the Super-Paging mechanism; however the algorithm suggested in this chapter does not suffer from this flaw and even utilizes the usual behavior of the paging mechanism to reduce the page fault rate. The algorithm actually makes use of the locality principle to prefetch base-pages that are a part of heavy used Super-pages and the results show that this prefetching makes the memory hit percents better.

We also aim at developing a good technique that finds the best page to be taken out when the page fault mechanism requires this in a Super-Paging environment based on all the available parameters. Here again the locality principle that the Super-paging environment induces helps us to select the victim page better, because if page’s neighbors have been accessed, it can imply that the page itself might be accessed as well and it may not be a good choice to swap the page out as the common base-page algorithms would have done.

The question of which page should be taken out also occurs in higher levels as well i.e. Which page should be in the cache and which page should be pointed to by the TLB. The algorithm suggested in this chapter can be also a good alternative for the well-known Clock algorithm in these decisions.

**SUPER-PAGES OF THE SUN MICROSYSTEM'S SPARC MACHINES**

We recently got a donation of a lab from SUN Microsystems, so our implementation is focused on this platform. In this section we detail the specification of the SultraSPARC CPU of SUN Microsystems and how this processor handles several sizes of page.

UltraSPARC CPU family is the main RISC CPU of Sun Microsystems server line. Multiple Page Size Support (MPSS) has been available by UltraSPARC CPUs since its first generation, but the support may vary between the UltraSPARC CPU family generations and even within one generation (mainly US-III) there might be a change in the support that this generation offers.

UltraSPARC I, II, III, IV cpu families supports 4 page sizes: 8KB, 64KB, 512KB, 4MB, whereas UltraSPARC IV+ supports 6 page sizes: 8KB,
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