On the Reliability of Post-CMOS and SET Systems

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ABSTRACT

The necessity of applying fault-tolerant techniques to increase the reliability of future nano-electronic systems is an undisputed fact, dictated by the high density of faults that will plague these chips. The averaging and thresholding fault-tolerant technique that has proven remarkable efficiency in CMOS is presented for SET-based designs. Computer simulations demonstrate the superiority of this fault-tolerant technique over other methods, which is specifically the case when an adaptable threshold is used. [Article copies are available for purchase from InfoSci-on-Demand.com]

Keywords: Fault Tolerance; Nanoelectronics Reliability; Redundancy; Single-Electron Transistor; Variability

INTRODUCTION

The advent of ubiquitous electronic appliances in the modern information society has founded its success on the premise of using highly reliable components in every development level. Based on the mature CMOS fabrication process, larger and faster, but also power-hungry and very complex integrated circuits have been fabricated on the assumption of very reliable operation of their constituting modules, from the atomic elements such as transistors, and passive components such as capacitances, routing lines, etc., to complex modules made of several thousands of transistors, such as arithmetic and logic units, memory blocks. Also, the availability of reliable electronic design automation (EDA) tools and efficient design-flows has been assumed.

The vast majority of microelectronic developments presented nowadays uses the well-established CMOS process and fabrication technologies which exhibit high reliability rates. The hypothesis of reliable components has mostly been adopted in the development of electronic systems fabricated in the past four decades. Several indicators show that future fabrication processes will exhibit increased failure rates and degraded fabrication yield. This paper focuses on the construction of reliable nanoelectronic systems made of intrinsically unreliable atomic
constituting elements. The main sources of faults are described in Section Reliability and Yield in Post-CMOS Fabrication Technologies. Section Techniques for improving reliability of Very Deep Sub-Micron (VDSM) and Post-CMOS devices focuses on currently applied methods for increasing design reliability. The averaging and thresholding technique is presented as a method enabling increasing the reliability of nanoelectronic systems, in Section Averaging and thresholding for increasing reliability. This work focuses on the specific case of single-electron transistor-based designs. The analytical framework of the averaging and thresholding technique using single-electron transistor-based designs is presented. The fault-tolerance of different realizations of the proposed averaging and thresholding technique is compared in Section Comparison of different fault-tolerant techniques, showing a significant improvement of fault resilience in all realizations.

RELIABILITY AND YIELD IN POST-CMOS FABRICATION TECHNOLOGIES

Some typical physical defects in VLSI chips include:

• Process defects - missing contact windows, parasitic transistors, oxide breakdown, etc.
• Material defects – bulk defects (cracks, crystal imperfections), surface impurities, etc.
• Aging defects - dielectric breakdown, electromigration, etc.

Errors are traditionally categorized into three main groups: permanent, intermittent and transient errors according to their stability and concurrence. Permanent errors are irreversible physical changes in a chip. The most common sources for this kind of errors are the manufacturing processes. Permanent errors also occur during usage lifetime of the circuit, especially when the circuit is old and therefore starts to wear out. Intermittent errors are occasional error bursts that usually repeat themselves every now and then, i.e. are not continuous as permanent errors. These errors are caused by unstable or marginal hardware, and are activated by environmental changes such as temperature or supply voltage change. Transient errors are temporal single malfunctions caused by temporary environmental conditions which can be external phenomenon such as radiation or noise originating from other parts of the chip.

Sources of errors can be classified according to the phenomenon causing the error. Such origins are for instance: the manufacturing process, physical changes during operation, internal noise caused by other parts of the circuit and external noise originating from the chip environment.

TECHNIQUES FOR IMPROVING RELIABILITY OF VDSM AND POST-CMOS DEVICES

Improving the reliability of CMOS has mostly been considered at device-level through several decades of size scaling. Fabrication technologies have included new materials, process recipes. The fabrication methodologies themselves have evolved and adapted to the new thinner sizes to be fabricated. Nevertheless, fabrication yield shows a significant decrease in very-deep submicron technologies. It is expected that the defect density in future nano-electronic systems be significantly higher than what is observed in current CMOS. Fabricating reliable systems from massively unreliable atomic devices is a challenge in the development of future multi-billion transistor system-on-chip.

Guidelines in the design of new hardware blocks have been used mostly to guarantee homogeneous design within a development group, and guaranteeing functionality by standardization of design techniques and methodologies. More recently, these ad-hoc techniques have started incorporating reliability directives at
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