Improving Switched Current Sigma Delta Modulators’ Performances via the Particle Swarm Optimization Technique

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ABSTRACT

This paper presents the optimal design of a switched current sigma delta modulator. The Multi-objective Particle Swarm Optimization technique is adopted to optimize performances of the embryonic cell forming the modulator; that is, a class AB grounded gate switched current memory cell. The embryonic cell was optimized regarding to its main performances such as sampling frequency and signal to noise ratio. The optimized memory cell was used to design the switched current modulator which operates at a 100 MHz sampling frequency and the output signal spectrum presents a 45.75 dB signal to noise ratio.

Keywords: Multi-objective Optimization, Particle Swarm Optimization, Sigma Delta Modulators, Signal to Noise Ratio, Switched Current Technique

INTRODUCTION

Oversampled analog-to-digital (A/D) converters are in good compatibility with digital VLSI technology. They become very popular and widely used in analog-to-digital conversion. In fact, this is mainly due to the following advantages (Medeiro, Perez-Verdu, & Rodriguez-Vasquez, 1999; Del-Rio, Medeiro, Perez-Verdu, Dela-Rosa, & Rodriguez-Vasquez, 2006):

- Oversampling and noise shaping techniques allow achieving accuracy that exceeds that of integrated circuit components;
- They relax requirements for anti-aliasing filters; they can be implemented with low order filters.

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In addition, by cascading oversampled modulators, A/D converters can achieve large resolution, robust operation and low sensitivity to non-ideal effects. An oversampling ΣΔ converter (Medeiro, Perez-Verdu, & Rodriguez-Vasquez, 1999; Del-Rio, Medeiro, Perez-Verdu, Dela-Rosa, & Rodriguez-Vasquez, 2006) (Figure 1) encompasses an anti-aliasing filter, a modulator and a decimator. Among the converter blocks, the modulator is the hardest to design (Norsworthy, Schreier, & Themes, 1997). Indeed, anti-aliasing filters can be simplified up to a simple RC low-pass filter, thanks to oversampling. The decimator is a digital block that can be optimally designed by means of widely available CAD tools (Del-Rio, Medeiro, Perez-Verdu, Dela-Rosa, & Rodriguez-Vasquez, 2006; Medeiro, Perez-Verdu, & Rodriguez-Vasquez, 1999; Norsworthy, Schreier, & Themes, 1997).

The modulator comprises many error mechanisms (Medeiro, Perez-Verdu, & Rodriguez-Vasquez, 1999), and performances of the converter highly depend on those of the modulator. Switched capacitor (SC) and switched current (SI) techniques have already been adopted for the design of such A/D converters (Del-Rio, Medeiro, Perez-Verdu, Dela-Rosa, & Rodriguez-Vasquez, 2006; Fakhfakh, Masmoudi, Tlelo-Cuautle, & Loulou, 2008; Loulou, Dallet, & Marchegay, 2000; Loulou, Dallet, Masmoudi, Marchegay, & Kamoun, 2004; Masmoudi, Fakhfakh, Loulou, Masmoudi, & Loumeau, 2007; Norsworthy, Schreier, & Themes, 1997; Oliaei, Loumeau, & Aboushady, 1997; Tan, 1997). Even though SI technique is not mature enough to cope with SC technique, advantages of the SI approach over those of SC make this technique very promising (Hughes, Worapishet, & Toumazou, 2000). Consequently, SI ΣΔ converters are excellent alternatives where much remains to be made (Fakhfakh, Masmoudi, Tlelo-Cuautle, & Loulou, 2008; Tan, 1997).

In this work we deal with designing high performance SI ΣΔ modulators. The main block of a modulator is the integrator. Performances of the later highly depend on those of the embryonic delay cell \((z^{-1})\) (Medeiro, Perez-Verdu, & Rodriguez-Vasquez, 1999; Del-Rio, Medeiro, Perez-Verdu, Dela-Rosa, & Rodriguez-Vasquez, 2006). Since a SI cell performs a half delay operation \((z^{-\frac{1}{2}})\), cascading two SI cells performs the full delay \((z^{-1})\). Thus, we mainly focus on optimizing performances of the SI memory cell regarding to its operating frequency and its precision (i.e. signal to noise ratio (SNR)). These performances are in conflict, i.e., maximizing one objective leads to the degradation of the other. Consequently, each performance has an individual optimal solution different from the other performance, then, a trade-off set of optimal solutions has to be found.

When dealing with “hard optimization” problems, analog designers make generally appeal to statistic-based approaches (Graeb, Zizala, Eckmueller, & Antreich, 2001; Medeiro, Rodriguez-Macías, Fernández, Domínguez-Astro, Huertas & Rodríguez-Vázquez, 1994). Performances of these approaches mainly rely on the experience of the designer, since the later fixes the operating point coordinates. These statistic-based approaches are time consuming and do not guarantee the convergence to the global optimum solution (Talbi, 2002).

Figure 1. Block diagram of a sigma delta A/D converter
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