Chapter 8

Full Adder Operation Based on Si Nanodot Array Device with Multiple Inputs and Outputs

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ABSTRACT

A highly functional Si nanodot array device that operates by means of single-electron effects was experimentally demonstrated. The device features many input gates, and many outputs can be attached. A nanodot array device with three input gates and two output terminals was fabricated on a silicon-on-insulator wafer using conventional Si MOS processes. Its feasibility was demonstrated by its operation as both a half adder and a full adder when the operation voltage was carefully selected.

INTRODUCTION

Recent progress in large-scale integrated (LSI) circuitry has been achieved by using metal-oxide semiconductor (MOS) field-effect transistors (FETs). Although MOSFETs are small and enable high performance, such as high current drivability, their integration into small chips is limited due to the huge power dissipation that results from high levels of integration (Chin & McAlister, 2005). In addition, their extremely small feature size (< 10 nm) results in various nanometer-scale fluctua-
tions in, for example, the surface and/or interface roughness, the impurity distribution, and the line edge roughness (Fukutome et al., 2006; Roy et al., 2006; Skotnicki et al., 2005). Controlling these fluctuations is quite difficult, so scaling down Si MOSFETs is problematic.

Single-electron devices (SEDs) are an attractive alternative for future LSI circuits because of their small size and very low power consumption. In contrast to MOSFETs, they can operate at low power because they can control the flow of a very small number of electrons (Grabert & Devoret, 1992; Kastner, 1993; Likharev, 1999; Ono et al., 2005; Takahashi et al., 2002; Wasshuber et al., 1998). However, this results in low current drivability, which generally makes it difficult to send the output signal to the next stage of the circuit. One way to overcome this is to use multiple-valued logic with cascode MOSFETs (Inokawa et al., 2001, 2002). This enables the device to output a voltage usable in conventional CMOS circuits. Many kinds of highly functional devices using multiple valued operations have been demonstrated (Degawa et al., 2004; Inokawa et al., 2003, 2004). The power consumption in the complicated circuits of these devices is reduced due to the use of multiple values. However, the reduction level is limited because the circuits also have to output high current to send the signal to the next logic stage. Ono et al (2002) proposed multibit adders in which the drain terminal of one single-electron transistor (SET) is directly connected to the source terminal of the next SET, and only the inputs and outputs are connected by wiring. This reduces the total wiring length in SED circuits although the capacitances of the source and drain terminals should be charged and then discharged on the basis of the signal transfer. In short, to achieve low power consumption, as many logic and/or arithmetic calculations as possible should be done in an SED network in which single-electron islands or SETs are directly connected to one another without wiring. A possible structure for this is the nanodot array. Moreover, with a nanodot array device, the nanodots can inherently couple with many input gates (Takahashi et al., 2002).

Size fluctuation is another challenge, not only in MOSFETs but also in SEDs. It is particularly challenging for SETs because the island size for practical SEDs will likely be smaller than the gate length of MOSFETs. Consequently, systems that can tolerate size fluctuation are needed. A previously proposed flexible nanodot-array device acts as a logic-function selectable device (Kaizawa et al., 2006). We have now obtained higher functionality by increasing the number of outputs and inputs. In addition, as a feasibility study, we fabricated a small nanodot array device with three input gates and two output terminals on a silicon-on-insulator (SOI) wafer and experimentally demonstrated its elementary characteristics as a half-adder and as a full adder.

**DEVICE CONCEPT**

Nanodot arrays should be the most effective structure for achieving low power consumption if we can implement high functionality. The larger the nanodot array, the more suitable it is for low power operation because the wiring is reduced more. Consequently, our ultimate goal is to build a very large nanodot array on which many input gates are attached so as to couple capacitively with many nanodots. It should also have many current output terminals because important, highly functional circuits, such as multibit adder circuits, generally need multiple outputs as well as multiple inputs.

Figures 1(a) and (b) show one possible structure for a nanodot array that has many gates and terminals. As illustrated in the diagrams, we can connect each output terminal to a different nanodot of the array. Since each gate couples capacitively with many dots, the voltage applied to each gate changes the electrical potential of the underlying dots, which induces current oscillation as a function of the gate voltage. However, the size