Chapter 1
Optimization of Linearity in CMOS Low Noise Amplifier

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ABSTRACT

In this chapter the authors evaluate a new and promising solution to the problem of power consumption based on “optimum gate biasing.” This technique consists in tracking the MOS operating region wherein the third derivation of drain current is zero. The method leads to a significant IIP3 improvement; however, the sensitivity to process drifts requires the use of a specific bias circuit to track the optimum biasing condition.

INTRODUCTION

The growing demand for wireless services has prompted the proliferation of many wireless standards. However, the wireless spectrum is a scarce resource and circuit designers have to put a particular effort in developing solutions that guarantee the various wireless standards to coexist. Spectrum crowding increases the number of interferers and this, in turn, degrades the overall performance of a wireless transceiver and put severe constraints on system linearity requirements. This chapter is specifically concerned with linearity issues in low-noise amplifiers (LNA’s). There are basically two sources of non-linear ties: device non-linear ties (characterized by the input compression point ICP1), and non-linear ties due to interferers (characterized by the input-referred third-order intercept point IIP3). The linearity of a transistor is directly connected to its current consumption: the larger the current the more linear the transistor. However, increasing the device bias current is not a practical solution in handheld or portable devices where low power consumption heavily constrains system’s specifications. Consequently, most of the state-of-the-art linearization
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Techniques aim at mitigating the effects of the intermodulation products, thus improving the IIP3. Two ways to improve LNA’s linearity are reported in the literature. One relies on a parallel feedback or feed forward path to compensate the non-linearities of the amplifier, the other uses ad-hoc compensation networks that require an thorough study of the amplifier topology in order to understand the mechanism that generates such non linearities. Nonetheless the major shortcoming of such techniques is their high power consumption that makes them unsuitable for low-power applications. The growing demand for more connectivity and service in wireless communication systems has brought out new challenges for circuit and system architectures. Among them is the management of a large number of communication standards in the radio part which requires frequency agility and high linearity. Indeed the various standards coexisting in the front-ends increase the number of interferers which degrade the overall system performances. Two building blocks are particularly concerned by such linearity purpose: the Power Amplifier (PA), in the transmitter, and the Low Noise Amplifier (LNA), in the receiver. However the linearity cannot be investigated with the same approach in these two kinds of amplifier. First, the PA is typically a large signal circuit where as the LNA is a small signal one. Furthermore the PA is the last stage of the transmitter, it is expected to provide a powerful output signal with good efficiency. The LNA, which is the first stage of a receiver, amplifies a weak signal collected by the antenna with the lowest noise as possible. In this chapter we focus on this last block.

The linearity is usually characterized by the input compression point (ICP1) and the input-referred third-order intercept point (IIP3). The first is the maximum input power for which a circuit behaves linearly at its fundamental frequency. The second estimates the cross modulations occurring in the circuit because of its non linear response. This last specification is directly concerned by the increasing number of standards in modern receivers. Led by low cost production and high yielding the development of wireless devices is supported by silicon technologies among them CMOS and BiCMOS are the most popular nowadays. The ultimate goal, pursued over a couple of decade, is the System On Chip implementation (SOC) which would definitely tackle the problems of multi chip integration. To address it pure CMOS solution is expected since digital makes the decision for the technology choice. As a matter of consequences RF CMOS concentrates many research efforts (Jussila et al., 2001) (Zargari et al., 2002) and especially the linearization of CMOS front-end.

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Two types of solutions aiming the improvement of the linearity in LNA are identified in the state of art. The first compensates for the non linearity occurring in the amplifier by a parallel feedback or feed forward path. It is rather a system approach performing high blocker rejection well suited for cellular phone applications. The feed forward principle is presented in the Figure 1(a), the time delay/multiplier chain generates a replica copy of the non linear term generated in the LNA that is cancelled at the output. The circuit is presented in the Figure 1(b), it is implemented in a 0.25µm CMOS technology and operates at 5GHz under 2V/22mW (Lin et al., 2006). In the Figure 2(b), a feedback solution is depicted (Werth, Schmits, & Heinen, 2009). The active cancellation filter