Chapter 5

Σ–Δ Fractional-N Phase-Locked Loop Design Using HDL and Transistor-Level Models for Wireless Communications

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ABSTRACT

This chapter presents a systematic design of a Σ-Δ fractional-N Phase-Locked Loop based on hardware description language behavioral modeling. The proposed design consists of describing the mixed behavior of this PLL architecture starting from the specifications of each building block. The description language models of critical PLL blocks have been described in VHDL-AMS, which is an IEEE standard, to predict the different specifications of the PLL. The effect of different noise sources has been efficiently introduced to study the overall system performances. The obtained results are compared with transistor-level simulations to validate the effectiveness of the proposed models in the frequency range around 2.45 GHz for wireless applications.

1. INTRODUCTION

The wireless communication market is undergoing a major expansion with the deployment of new technologies and standards opening the prospect of significant impacts in many application areas (security, health, automotive, environment, cold chain management, manufacturing, telecommunications, robotics, etc.). The emerging wireless technologies require architectures with reduced complexity, cost and power consumption; however, they require specific circuits with more accuracy and best performance.

DOI: 10.4018/978-1-4666-0083-6.ch005
The design of state-of-the-art wireless is a challenging task transceivers since many design constraints must be considered, for this reason mixed-signal CAD (Computer- Aided Design) tools are necessary to explore the design space quickly and efficiently. Currently, hardware description languages are widely used in the design of mixed-signal circuits. Indeed, the VHDL-AMS standard allows the implementation of the top-down hierarchical approach for analog and mixed systems (Peterson, 2002). Therefore, it can be used straightforwardly for behavioral modeling and design of a phase locked loop (PLL), which is a key element for any wireless communication system (Hinz, 2000).

With the demand among different applications, standard PLL frequency synthesizers with integer-N dividers must offer a fast-settling time, a good noise performance, and an accurate frequency resolution. Usually, due to the tradeoff between loop bandwidth and channel spacing, fractional-N PLL is a better candidate than integer-N PLL (Riley, 1993). Thus, the fractional-N technique offers wide bandwidth with narrow channel spacing and relaxes PLL design constraints for phase noise (Riley, 2003). The Σ-Δ fractional-N PLL is an attractive solution for agile frequency synthesis or direct modulation schemes (Perrott, 1997).

In this chapter, a Σ-Δ fractional-N PLL is modeled using VHDL-AMS and synthesized for wireless applications. For this study, many HDL models have been studied and tested for different PLL blocks. The VCO and Σ-Δ modulator are the major blocks that affect the PLL phase noise. These blocks are efficiently described and simulated in VHDL-AMS to estimate the PLL phase noise. The proposed PLL models use ELDO scripts (Mentor Graphics, 1998) mixed with VHDL-AMS models which allow the simulation of some PLL blocks at transistor-level and others at behavioral level. Several jitter noise sources are studied based on different noise models (Kundert, 2001) and included into the PLL model to investigate non-ideal effects. These mixed behavioral models enable a fast simulation of the Σ-Δ synthesizer and an accurate phase noise prediction. A comparison with transistor-level simulations validates the proposed models.

The chapter is organized as follows. Section 2 presents the role of the frequency synthesizers in the radio transceivers. Section 3 gives a review about the frequency synthesis techniques. Section 4 describes the fractional-N PLL. Section 5 presents the behavioral models of the PLL building blocks. The PLL system-level design is discussed in section 6. The PLL specifications and the behavioral modeling of noise in PLL are outlined. The system-level simulations results are given in section 7. Finally, section 8 presents the conclusion and some perspectives on future research directions.

2. FREQUENCY SYNTHESIZERS IN RADIO TRANSCEIVERS

The evolution of radio transceiver architectures is derived by the explosive development of standards and applications for wireless communications. Since the first superheterodyne radio receiver presented by Edwin H. Armstrong in the 1920’s (Armstrong, 1924), several transceiver architectures have been developed and reported in the literature (Razavi, 1998). The main differences between these topologies concern the implementation techniques of the receiver and the transmitter parts. However, the purpose remains the same. Indeed, the wireless transceivers must be able to generate a wide range of frequencies in order to upconvert the outgoing data for transmission and downconvert the received signal for processing (Lee, 1998). Hence, frequency synthesizers are widely used in modern radio communication systems.

Figure 1 shows an example of superheterodyne receiver which is the most commonly used receiver architecture. The received signal is down mixed to two intermediate frequencies (IF) before it is con-
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