Chapter 11

Design and Implementation of Hardware Modules for Baseband Processing in Radio Transceivers: A Case Study

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ABSTRACT

In this chapter, the main aspects of the design of baseband hardware modules are addressed. Special attention is given to word-length optimization, implementation, and validation tasks. As a case study, the design of an equalizer for a 4G MIMO receiver is addressed. The equalizer is part of a communication system able to handle up to 32 users and provide transmission bit-rates up to 125 Mbps. The word-length optimization process will be explained first, as well as techniques to reduce computation times. Then, the case study will be presented and analyzed, and the different tasks and tools required for its implementation will be explained. FPGAs are selected as the target implementation technology due to their interest from the DSP community.

DOI: 10.4018/978-1-4666-0083-6.ch011
1. INTRODUCTION

The design of communication systems is a challenging task that includes many complex stages. It requires performing accurate simulations of the hardware involved along with the physical environment (modeling of radio channels, analog circuitry with corresponding non idealities, etc.), designing hardware for both analog and digital blocks and testing the final implementation in a realistic framework.

In radio communications, baseband processing refers to the algorithms applied to the useful signal, previously to carrier modulation. Nowadays, it is usually carried out digitally by applying sometimes very complex or computation-intensive Digital Signal Processing (DSP) techniques. Depending on the considered transmission scheme, it can include algorithms for Fast Fourier Transforms (FFT), time and frequency synchronization, channel estimation and equalization, channel coding and decoding, correction of front-end impairments, etc.

This chapter is focused on the development tasks performed for the design, implementation and validation of a Fourth Generation (4G) MIMO communication system in the framework of the European Project 4MORE (Stefan Kaiser et al., 2004). Baseband processing was able to provide the high data rates and spectral efficiency expected from 4G wireless multi-user communication systems, merging state-of-the-art techniques, as multiple antennas (MIMO), with MC-CDMA and other advanced signal processing methods. Additional details and references on these topics will be provided in Section 4.

The complexity of the digital signal processing involved in baseband processing imposes the use of dedicated hardware that can handle the computation power by means of highly parallelized architectures. The preferred target technologies are ASICs and FPGAs. The first ones provide the best performance at a cost of very long and expensive design cycles. The latter ones, originally intended for prototyping, still provide good performances with reduced design cycles and, for that reason, they have been massively used during the last decade. Basically, FPGAs are composed of thousands of configurable logic blocks (LUTs: look-up tables) that can be programmed and interconnected at pleasure, as opposed to ASICs, where the architecture cannot be modified after manufacturing. Once a suitable digital architecture is envisioned by the designer, available commercial tools handle most of the optimization tasks required to obtain high-performance architectures. Thus, the design cycle is highly reduced.

In order to keep the cost of the hardware system (i.e. area and power consumption) to practical bounds, it is necessary to translate the original floating-point description of the algorithms to fixed-point arithmetic, which is more suitable for high-speed and low-power systems. This translation is known as quantization and it aims at finding the minimum precision that the mathematical operation requires to reduce cost, while matching the application quality standards. Reducing the precision implies decreasing the number of bits of each signal (word-length) and, thus, reducing the silicon area and power consumption of the arithmetic operators. Once the word-lengths are determined, the hardware designer must deal with the architectural issues. Several optimizations can be applied in order to produce an efficient implementation of DSP algorithms (pipelining, parallelization, etc.) with the help of electronic design tools.

In this chapter, we present the main tasks involved in the digital design of baseband modules and illustrate them with a case study. Special attention is given to the process of Word-Length Optimization (WLO), as this task is very time-consuming due to a lack of a clear methodology and to the use of simulation-based approaches. A methodology for fast WLO is presented. Then, the complete design of a channel equalizer is addressed. The tools used, as well as the engineering decisions taken, are explained, to provide