High Throughput Realization of a New Systolic Array based FFT using CORDIC

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ABSTRACT

In this paper, the authors propose a new systolic array for radix-2, N-point discrete Fourier Transform (DFT) computation based on CORDIC (CO-ordinate Rotation Digital Computer). Complex multiplication can be done by this in a rather simple and elegant way. A CORDIC based multiplier less DFT architecture is designed in order to improve the performance of the system. It is able to provide two transforms per each clock cycle. The proposed design is well suited for high speed DSP-applications.

Keywords: CO-Ordinate Rotation Digital Computer (CORDIC), Digital Signal Processing, Discrete Fourier Transform (DFT) Computation, Systolic Array, Telecommunication

1. INTRODUCTION

The Discrete Fourier transform is one of the major tools in the field of digital signal processing. Many advanced telecommunication systems, e.g. Wireless LAN (HIPERLAN/2), Digital Subscriber Line (DSL), Power Line Communication (PLC), Terrestrial Integrated Services Digital Broadcasting (ISDB-T), Digital Video Broadcasting Terrestrial (DVB-T) and possibly 4th generation mobile phones, use Coded Orthogonal Frequency Division Multiplexing (COFDM) as a modulation scheme, which is based on the FFT-algorithm (Mondwurf, 2002). Since the DFT requires intensive computation so there is a great demand to develop fast DFT processors to meet real time signal processing requirements. In some previous years, systolic array technique has been come in the field of VLSI and lots of work has been done on that. Because such architectures have the features of regularity, modularity, concurrency and high performance those are quite important for the efficient low cost VLSI implementation. So many linear systolic array designs have been presented which require N-clock cycles to compute N-point DFT. Among them, the architectures listed in (Chang & Wu, 1988; Beraldin, Aboul-nasr, & Steenaart, 1989; Murphy & Swamy, 1994) needed N complex multipliers, and corresponding hardware circuitry looks quite impractical for large value of N. Although the array proposed by Choi and Boriako (1992) occupies only $\log_2 N$ complex multipliers, but still

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needs $N \log_2 N$ delay elements for intermediate data storage and switching elements those were very complex for higher point DFT. To eliminate these more hardware and switching difficulties, Ching et al. (2000) suggested a new architecture based on a radix-2 fast algorithm, which still consumes $\log_2 N$ complex multiplier and is able to provide a throughput of one transform sample per clock cycle. In contrast to previous design Chao Cheng has come with architecture (Cheng & Parhi, 2007), as compared to last one this radix-2 based design have double throughput with slightly changed in hardware.

Unfortunately, In all the above mentioned architectures they consist complex multiplier as one of the important part of the entire circuit, to compute DFT. Computational complexity of this multiplier is generally much high and this is not useful for high throughput VLSI implementation. So in this paper, we present a new DFT architecture which is completely multiplier less and throughput rate is also high as compared to all the structures, discussed earlier.

This paper is organized as follows. Review of the FFT-Algorithm is presented in section 2. Discussed about CORDIC technique is summarized in section 3. Proposed new design is in section 4. Finally we end up our paper with comparison and analysis of proposed architecture by some existing architectures and conclusion respectively in section 5 and section 6.

2. THE ALGORITHM FOR FFT-COMPUTATION

Firstly we take review of the FFT-algorithm presented in (Choi & Boriakoff, 1992). Now N-point DFT is defined by:

$$y_k = \sum_{n=0}^{N-1} x_n W_n^{nk}, \quad k = 0, 1, 2, \ldots, N - 1 \quad (1)$$

where N is a power of two and twiddle factor $W_N = \exp(-j2\pi / N)$.

We can also rewrite above equation as follows

$$Y = W(N)X \quad (2)$$

where

$$Input \ vector \ X = [x_0, x_1, x_2, \ldots, x_{N-1}]^T$$

$$Output \ vector \ Y = [y_0, y_1, y_2, \ldots, y_{N-1}]^T$$

and transformation matrix

$$W(N) = \begin{bmatrix}
1 & 1 & 1 & \ldots & 1 \\
1 & W_N^{2x1} & W_N^{1x2} & \ldots & W_N^{1(N-1)} \\
1 & W_N^{2x1} & W_N^{2x2} & \ldots & W_N^{2(N-1)} \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
1 & W_N^{(N-1)x1} & W_N^{(N-1)x2} & \ldots & W_N^{(N-1)(N-1)}
\end{bmatrix} \quad (3)$$

By using property $W_N^{nk} = (-1)^k W_N^{(m+n/2)k}$, we can partition the matrix W(N) into four quadrants. To do that we need to shift of all its even numbered rows in upper half, which can be accomplished by multiplying both sides of (2) by permutation matrix $Q(N) = [e_0, e_1, e_2, \ldots, e_{N/2}, e_1, e_2, \ldots, e_{N/2}]^T$, where $e_n$ is unit $N \times 1$ column vector in which $N + 1$ element is 1.

$$Q(N)Y = Q(N)W(N)X \quad (4)$$

where E(N/2) and D(N/2) are given by (5) and (6) respectively.

$$E(N/2) = \begin{bmatrix}
1 & 1 & 1 & \ldots & 1 \\
1 & W_N^{2x1} & W_N^{1x2} & \ldots & W_N^{1(N/2-1)} \\
1 & W_N^{2x1} & W_N^{2x2} & \ldots & W_N^{2(N/2-1)} \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
1 & W_N^{(N/2-1)x1} & W_N^{(N/2-1)x2} & \ldots & W_N^{(N/2-1)(N/2-1)}
\end{bmatrix} \quad (5)$$
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