Design Flow for Silicon Chip Implementing Novel Platform Architecture for Wireless Communication

Prabhat Avasare, IMEC, Heverlee, Belgium
Jeroen Declerck, Bird and Goen, Leuven, Belgium
Miguel Glassee, IMEC, Heverlee, Belgium
Amir Amin, IMEC, Heverlee, Belgium
Erik Umans, IMEC, Heverlee, Belgium
Praveen Raghavan, IMEC, Heverlee, Belgium
Martin Palkovic, IT4Innovations, Ostrava, Czech Republic

ABSTRACT

In current era of complex chip designs targeting wireless mobile terminals, architects and designers need to conform to tight design constraints – both in terms of performance (e.g., execution time, silicon area, energy consumption) and time-to-market. Further, additional flexibility is required in these designs to handle multiple wireless standards, sometimes even concurrently. To achieve these challenging goals, the authors introduce a platform architecture that uses a decentralized control to minimize communication and control overhead while keeping timing predictable by using state-of-the-art components and a novel interconnect. The authors demonstrate three main achievements in running multiple wireless standards on their platform: 1.053Gbps 4x4 80MHz WLAN 802.11ac receiver data path meeting the SIFS timing with a latency of 12.5μs, dual concurrent 173Mbps 2x2 20MHz Cat-4 3GPP-LTE receiver and platform reconfiguration from WLAN 11n receiver to 3GPP-LTE one in 52μs. Further the authors describe the design flow used to prepare main components of our platform architecture for a tape-out, while especially keeping a close eye on energy consumption. We believe that our chip design flow is generic and can be used in other custom processor chip designs even outside wireless domain.

Keywords: Design-Flow, Energy Estimation, Platform-Based Design, Silicon Implementation, Wireless Communication

DOI: 10.4018/jertcs.2013010103
1. INTRODUCTION

Wireless communication requires continuous development of new standards to satisfy ever increasing user demands. This is true not only for cellular standards (e.g. GSM, WCDMA, HSDPA, 3GPP-LTE) but also for other wireless standards (e.g. WiMAX, WLAN, DVB-H, DVB-T2). There is a challenge to implement these standards power-efficiently with mandated latency and throughput constraints. Additionally, there are design costs (cost of used resources, silicon area) and time-to-market constraints. Especially, NRE (Non-Recurrent Engineering) costs associated with the design and tooling of such complex chips are growing rapidly. One universally adapted solution to tackle such challenging goals is platform-based design (Sangiovanni, 2001). A platform-based design typically uses a mix of programmable and full custom ASICs to achieve flexibility, extensibility in design and at the same time a good control over all design costs. Additionally, a systematic platform-based design flow is developed to start from application algorithms and end in a mapping on a silicon chip – either dedicated custom-ASIC or a programmable processor. This way, platform-based design can trade-off various components of manufacturing and design costs while sacrificing as little as possible on potential design performance.

In our design approach for wireless mobile terminals, we have used platform-based design based on reprogrammable radio architectures (broadly referred as Software Defined Radio). In this paper, we discuss mainly two aspects: the architecture of the platform and the design flow used in taking the platform architecture to tape-out. Discussion about design flows for mapping applications on such platforms can be found in (Palkovic, 2010).

In terms of implementation of wireless standards, in this paper we mainly focus on the baseband part in the receive path of the physical layer (PHY). A typical implementation architecture for such a receive path contains a Digital Front-End (DFE), BaseBand Engine (BBE) and Outer MoDem (OMD). Most of the wireless platform architectures available today emphasize on the BBE which performs the computation-intensive inner modem processing. However, we believe that equal attentions should be given to two more aspects: interconnect between components and overall control flow. In this paper, we introduce a platform architecture that uses decentralized control and a novel interconnect between state-of-the-art components (ASICs and Domain Specific Instruction Processors, DSIPs) to minimize communication and control overhead. With our architecture we have made three key achievements. First, our platform can support multiple wireless standards (WLAN, 3GPP-LTE, DVB-T2) achieving mandated latency and throughput constraints. Second, with our architecture, we can run two concurrent and independent data streams. And third, we can switch among different wireless standards within an order of 100μs. This paper describes first the platform architecture and then design flow used to take this platform architecture towards a tape-out. The main contribution in our design flow is the attention given to early energy consumption estimation.

What exactly is the problem in managing energy consumption during chip designs? Here we are not referring to the low power techniques to reduce energy consumption, but more on how to manage these different techniques and percolate their effects at the application mapping level so as to get an early estimate of power consumption e.g. wireless application designer is always interested in knowing how much energy is consumed by his/her algorithm during a complete packet processing. There is always a trade-off between accuracy of simulation and simulation time – the more accurate simulation (e.g. gate-level or netlist-level simulation) takes many orders of magnitude more resources than a cycle-accurate Instruction Set Simulator (ISS)-based simulation. Moreover there is usually a large effort involved to map an application from a cycle-accurate level down to gate-level simulations. Typically in a design flow targeting a tape-out starting from a design, initially when the software application is mapped on a design...
Modeling Communication in Multi–Processor Systems–on–Chip Using Modular Connectors
www.igi-global.com/article/modeling-communication-multi-processor-systems/42984?camid=4v1a

Conceptual Model for Examining Consumer Broadband Adoption, Usage, and Impact
www.igi-global.com/chapter/conceptual-model-examining-consumer-broadband/6963?camid=4v1a